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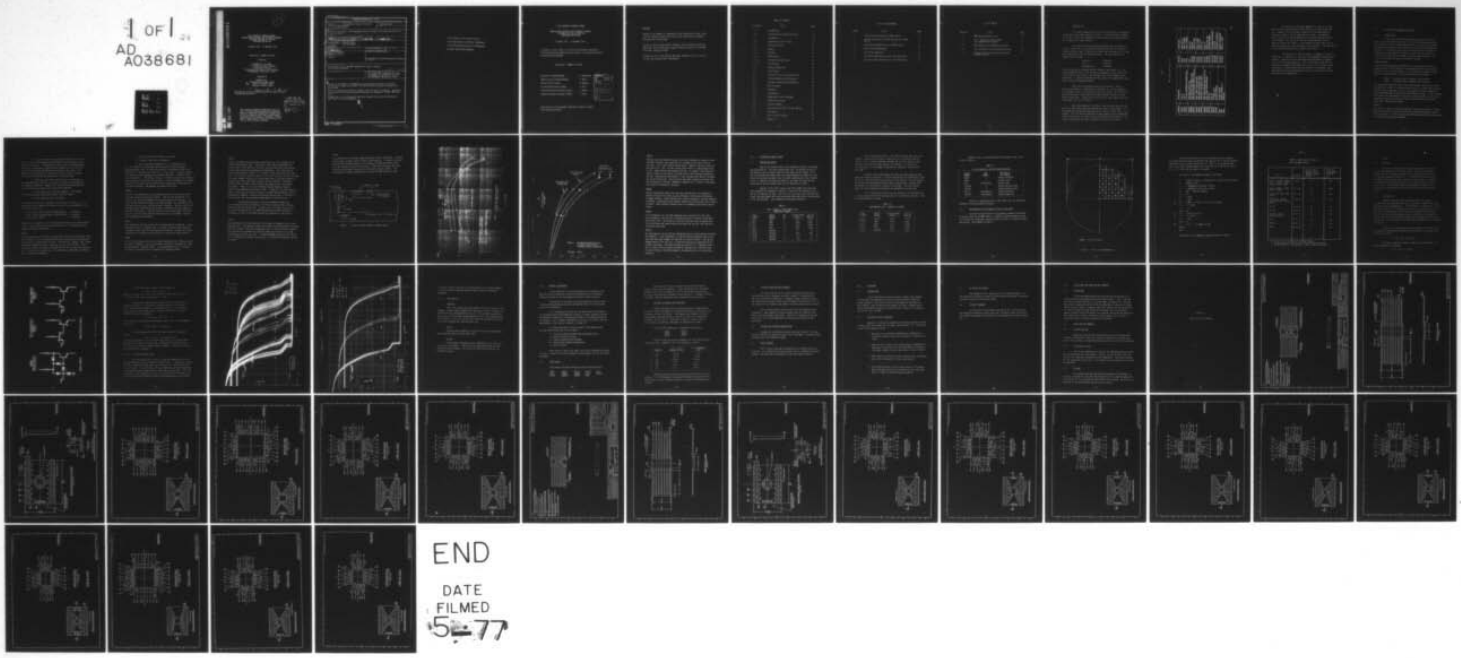

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SIXTH QUARTERLY PROGRESS REPORT
MANUFACTURING METHODS AND TECHNOLOGY PROGRAM
FOR BEAM LEAD SEALED JUNCTION
SEMICONDUCTOR DEVICES

21 August 1976 - 21 November 1976

Contract No. DAAB07-75-C-0033

Placed By

DEPARTMENT OF THE ARMY
U. S. Army Electronics Command
Production Division
Procurement and Production Directorate
Fort Monmouth, New Jersey 07703

Prepared By

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13. ABSTRACT

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Results on the discrete devices, however, have not been as promising. Additional lots of each device type are being processed in an attempt at further improving yields.

Packages for all of the devices have been designed for use in satisfying the qualification test requirements.

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SIXTH QUARTERLY PROGRESS REPORT

MANUFACTURING METHODS AND TECHNOLOGY PROGRAM FOR BEAM LEAD SEALED JUNCTION SEMICONDUCTOR DEVICES

21 August 1976 - 21 November 1976

The object of this study is to refine the processes required to fabricate beam lead sealed junction devices in production quantities by manufacturing methods.

Contract No. DAAB07-75-C-0033

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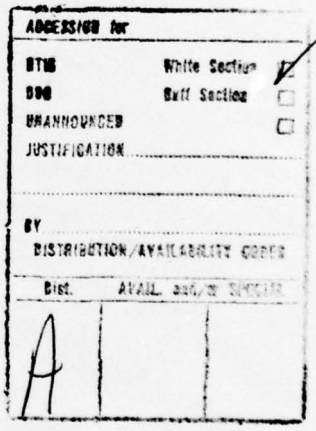

ABSTRACT

Because of the number of integrated circuits processed to date, along with the favorable probe yield results, the 5400 and 54LS processes have been well established.

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1.0 INTRODUCTION

This report summarizes the activities during the sixth quarter of Motorola's beam lead contract with the U. S. Army Electronics Command. All of the discrete and integrated circuit devices being manufactured on this program are listed in Table I.

The purpose of this manufacturing methods and technology contract is three fold: 1) to make these devices available for military/industry systems usage; 2) optimize the beam lead technology; and 3) lower beam lead product costs by improving yields. The yield goals of the program are as follows:

Discretes	-	20 percent
IC's	-	10 percent
60 Gate Array	-	5 percent

These yield goals are defined quite differently than normal, i.e., die start through die ship. This includes any breakage or loss at any step in the process from initial oxide through final die high power visual inspection. It should be pointed out that these yield requirements apply only to the pilot production phase.

There are three primary phases of the program: Phase I - Engineering, Phase II - Confirmatory, and Phase III - Pilot Production. At the present time all of the devices listed in Table I are in Phase II with the exception of the 54LS193, 54LS194, 54LS196, 54LS197, and the RA108 60 Gate Array. These devices, which are far more complex than the other types, are still in Phase I.

When the program was initiated, it was believed that the 54LS devices and the gate array would present the major yield problems. No redesigned gate arrays have been delivered to date, so that yield is still unknown. The 54LS devices processed to date, however, have yielded more than satisfactorily, at least as far as processing and DC probing is concerned, with some device types yielding in excess of 60 percent.

TABLE I

MM&T BEAM LEAD DEVICE LIST

DEVICE	FUNCTION	DEVICE	FUNCTION
1N746	3.3V Z	5405	HEX INV O.C.
1N748	3.9V Z	5410	TRIP 3 NAND
1N5314	5.14 ma CURRENT SOURCE REG.	5440	DUAL 4 NAND
2N2484	NPN HIGH GAIN (100)	5473	DUAL JK
2N2907	PNP SWITCH AND AMPLIFIER	54LS04	HEX INV
2N3251	PNP HIGH SPEED SWITCH (200 ns)	54LS08	QUAD 2 AND
2N3467	PNP 1 AMP CORE DRIVER	54LS21	DUAL 4 AND
2N3501	NPN HIGH VOLTAGE (150V)	54LS32	QUAD 2 OR
2N3635	PNP HIGH VOLTAGE (140V)	54LS73	DUAL JK
2N3639	PNP HIGH SPEED SWITCH (20 ns)	54LS74	DUAL D
2N3725	NPN 1 AMP CORE DRIVER	54LS86	QUAD 2 EX OR
2N3960	NPN RF	54LS138	DECODE-DEMUX
2N4260	PNP RF	54LS193	UP-DOWN COUNTER
2N5115	P CHAN JFET	54LS194	4 BIT S.R.
RA108	60 GATE ARRAY	54LS196	DECADE COUNTER
5400	QUAD 2 NAND	54LS197	BINARY COUNTER
5401	QUAD 2 NAND O.C.	54LS253	DUAL 4-1 MUX
5404	HEX INV		

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By contrast, it has been somewhat of a surprise to learn that the discretes have been far more difficult to process than the IC's. However, this has primarily been due to the requirement of yielding to specific device types within a family. An example of this, as outlined in the introduction of the Fifth Quarterly Report, is the 1N5314. This device is only one of approximately thirty regulators within the family. On one recently probed sample, half of these various devices could be found on the same wafer. This was only for Ip, the primary characteristic probed at that step.

The status of all the discretes is reviewed in Section 2.0 and the IC's in Section 3.0. Section 5.0 and Appendix A should be of interest, since they discuss the design and development of packages for all of the required devices. This is important, since there is presently no method of performing electrical or life testing on beam lead devices. However, beam lead chip carriers are presently under development by several manufacturers for use in electrically testing the devices over temperature.

2.0 DISCRETE DEVICE PROCESSING STATUS

2.1 INTRODUCTION

It has been pointed out many times previously (the latest being in the conclusions of Section 4.0 of the Fifth Quarterly Report) that processing of only three engineering lots of each discrete device type was both unrealistic and insufficient for establishing production processes. As reviewed in this section, because of the difficulty in targeting-in on the specific discretes in each family of devices, in several cases additional confirmatory lots had to be processed. The results of each device type are reviewed as follows:

1N746 and 1N748

A new technique employing the addition of a 3-micron thick intrinsic epitaxial layer on the surface of the starting material was utilized on two lots of each of these devices. This procedure eliminates the base photo step and diffusion. The following yields were obtained:

1N746 - 24 percent and 8.5 percent, 4221 good die
1N748 - 33 percent and 8.8 percent, 3144 good die

This processing technique reduced the diode leakage current by one order of magnitude; therefore, no appreciable failures for leakage were observed. The main failure mode was V_Z and Z_Z; some wafers which were probed and failed the 1N746 specification could have passed as 1N748. It was interesting to note that the change of resistivity across the wafer is still contributing to yield loss since portions of each wafer meet 1N746 while others meet 1N748 specifications.

1N5314

This device is one of 32 current regulators normally processed as a family. Material and process technologies have made considerable progress during the last quarter. In order to gain some reasonable control over the process, the following procedure was adopted:

1) The gate diffusion can only be calculated to one's best ability, since no measurements on individual die are possible at this step in the process. Consideration is being given to redesigning the mask set to incorporate a process control pattern in the scribe grid area for test probing and tweaking the process at this step. This change, if incorporated, will not affect the basic device structure since it will be outside the perimeter or in the grid area.

2) After the source-drain photo resist was completed it was hoped that the variation in I_p across the wafer could be measured and tweaked accordingly. However, this could not be accomplished due to high contact resistance at the source-drain openings.

3) After source-drain diffusion, however, a low contact resistance was established and the wafers could be tweaked.

4) Final tweak was done at pre-ohmic.

The yields of the first lot processed this way were as follows. (It is important to note, however, that these yields are to one parameter on the specification only, I_p.)

I_p lot yield to entire family (1N5283-1N5314)	=	76 percent
I_p lot yield to proposed family (1N5310-1N5314)	=	42 percent
I_p lot yield to 1N5314	=	20 percent

Probing to all parameters, this lot yielded 27 percent to the 1N5310-1N5314 family. These results are very encouraging, but it is believed that this cannot be repeated consistently.

2N2484

Five confirmatory lots have been rejected and a detailed investigation showed the following: prior to emitter diffusion the collector-base breakdown was well defined as greater than 130 volts. After emitter, however, this voltage dropped to between 40-60 volts resulting in a C_{EO} of 20-30 volts. Both C_{BO} and C_{EO} require a voltage of greater than 65 volts to meet the specification. Re-examining the processes, the following was determined and changes were subsequently introduced:

1) Epi resistivity and thickness is correct.

2) Collector diffusion is acceptable.

3) The present base diffusion of ρ_s = 300 ohms/sq. and X_j = 3.1 microns is not the most desired cycle for high efficiency. When supporting a C_{BO} = 65 volts the spread of the depletion layer into the base is of the order of 0.95 micron. This figure is equal or greater than the base width requiring an h_{fe} greater than 200. A new base cycle was designed of ρ_s = 200 ohms/sq. and X_j = 2 microns resulting in a depletion layer spread of 0.54 micron into the base. A new confirmatory lot has been started into the wafer area and the previous assumption has been verified at emitter diffusion. No problems occurred at that step.

2N2907A

The first confirmatory lot had a good probe yield at final test with the exception of V_{CE} (sat) at high currents. The lot was rejected for this reason. The second confirmatory lot was also rejected for low h_{fe}. The third lot was rejected at emitter for punch-through. All confirmatory lots indicated that V_{CE} (sat) at high current is marginal. Based on these findings, and further calculations, the collector diffusion time was increased from 60 to 120 minutes. This new time will bring the collector diffusion more in line with similar PNP epi thickness such as the 2N3467. No more major problems are anticipated.

2N3251

One confirmatory lot had a yield of 4.5 percent but not enough die. A new confirmatory lot is in process now. Collector diffusion times have been increased to meet V_{CE} (sat) requirement more readily. No gold or platinum diffusion will be used since the previous lot met all AC specifications.

2N3467

The first confirmatory lot which yielded 7 percent had a Pt diffusion prior to contact diffusion. Four of the 8 wafers had 200 to 330 good die. Main failure mode was leakage current. A new confirmatory lot is in process including a gettering cycle to overcome this leakage problem.

2N3501

Three confirmatory lots have been rejected for V_{CE} (sat) problems, high current beta and beta kink. Calculations have clearly shown that the emitter area of this device is too small to avoid operating in the region of non-linear mobility and conductivity modulation. This causes the so-called beta kink, which results in a failure of high current V_{CE} (sat) and beta. The Discrete Production Group is using the same area and have the same beta kink, however, the R_{sat} is so much lower (due to collector contact to bottom of die) that their specifications are not affected. Even with a 10 hour diffusion time in the collector, the penetration is only about 20 microns. Figure 1 is a cross-sectional drawing showing a typical structure with appropriate resistor values. To meet all V_{CE} (sat) requirements, a total R_{sat} less than 2.6 ohms is required meaning that R_2 must be substantially reduced. Increasing diffusion time in excess of 10 hours is not practical since the substrate doping begins to affect the epi.

One potential solution is having a phosphorus doped plug in the substrate which out-diffuses into the Epi and meets the collector diffusion from the top half way. Figures 2 and 3 are beta versus I_C and V_{CE} (sat) characteristics of a 2N3501 processed by standard production techniques, as well as two beam lead devices diffused at 3 and 8 hours.

2N3635

Two confirmatory lots were rejected for low BV_{CEO} and BV_{CBO} as well as very high V_{CE} (sat). The second lot which had a much increased collector diffusion time still failed. Both lots looked good prior to the Pt diffusion; however, the Pt diffusion destroyed the collector properties reflecting in a high leakage BV_{CEO} and high V_{CE} (sat). A similar argument applies to this device as to the 2N3501 with respect to beta kink. No further confirmatory lots are in process.

2N3639

The confirmatory lot has been completed with a yield of 82 percent. Five and a half wafers yielded a total of about 15,000 good die. Collector diffusion time has been increased from 35 to 60 minutes, thereby overcoming slight V_{CE} (sat) problems occurring in the past. Probe yield was very consistent and uniform from wafer-to-wafer which reflected a mature process. This represented the highest yielding lot on any of the MM&T devices to date.

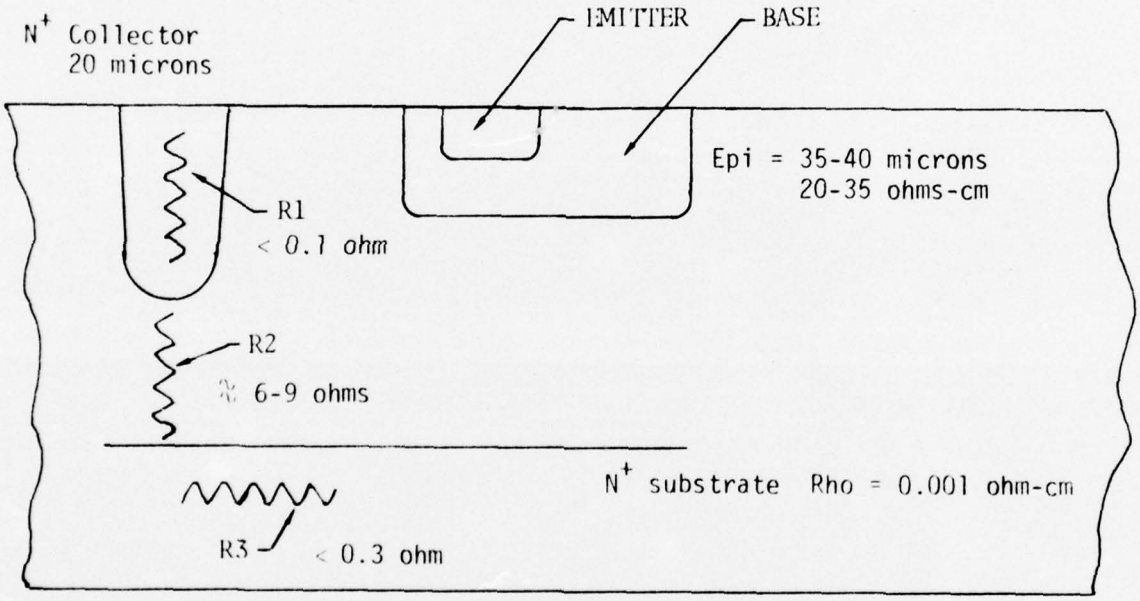


FIGURE 1 - Cross-sectional Drawing of 2N3501 Device

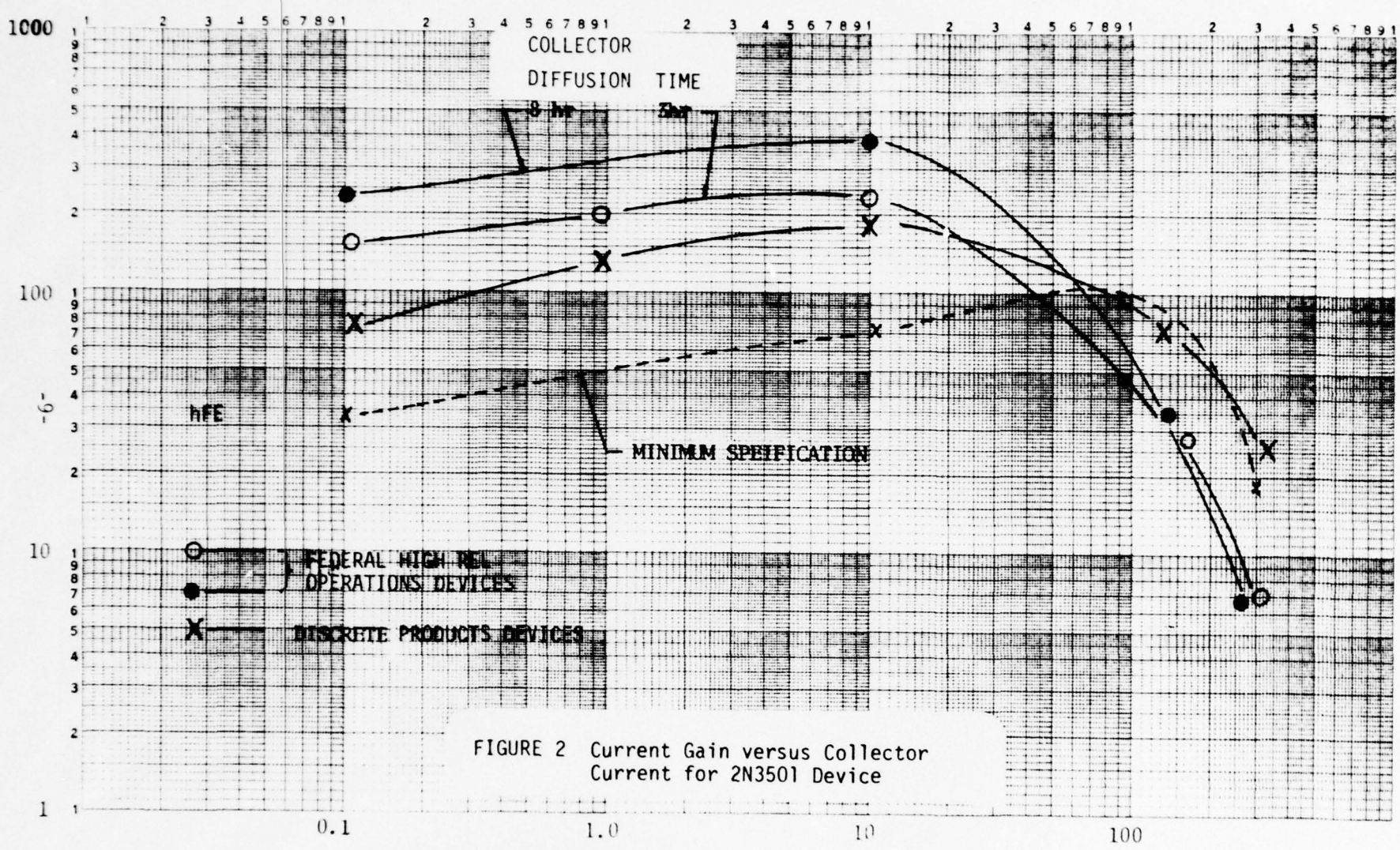


FIGURE 2 Current Gain versus Collector Current for 2N3501 Device

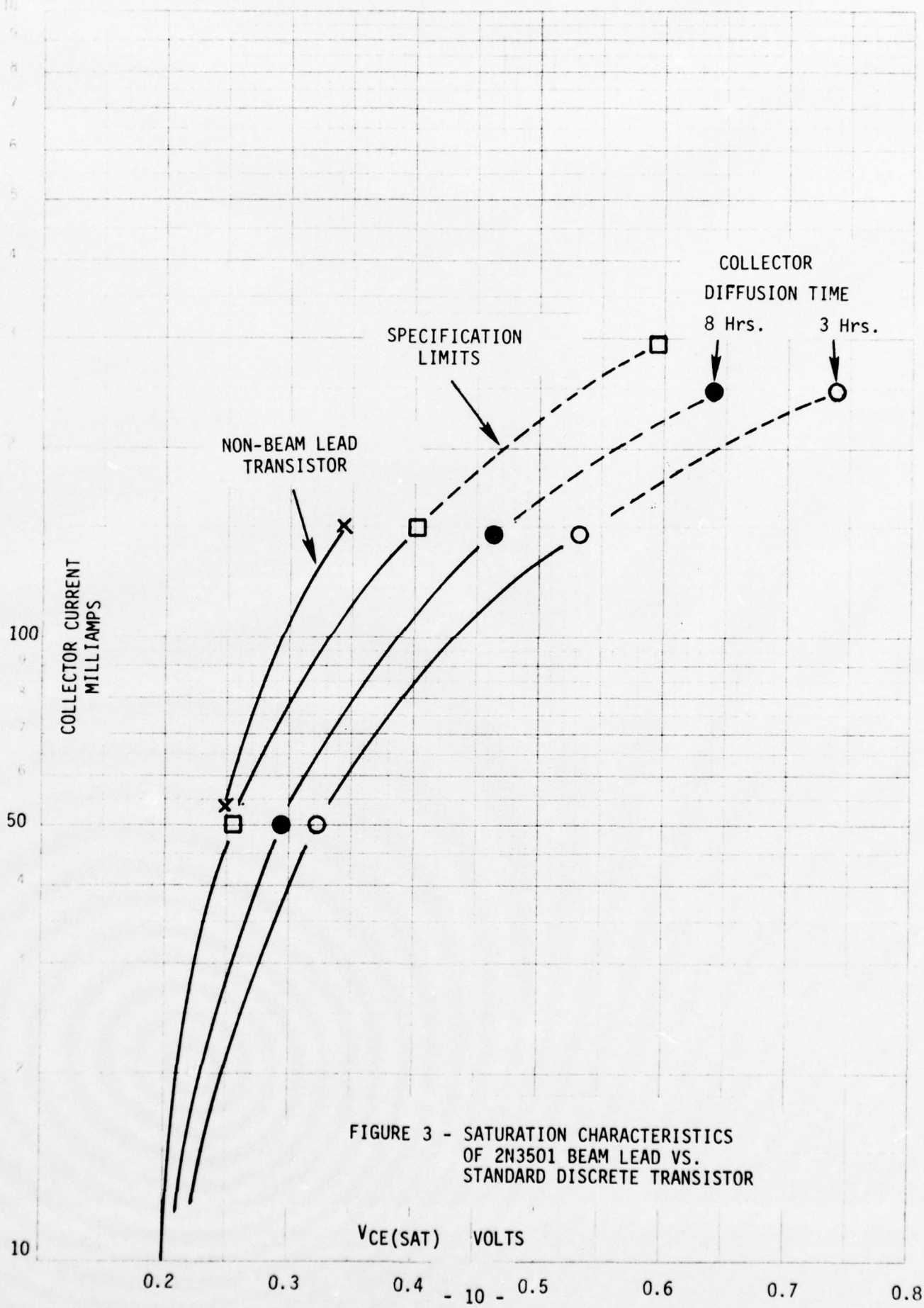


FIGURE 3 - SATURATION CHARACTERISTICS
OF 2N3501 BEAM LEAD VS.
STANDARD DISCRETE TRANSISTOR

2N3725

Previous lots were marginal on V_{CE} (sat) which prompted an increase in the collector diffusion time resulting in a voltage of less than 0.45 volt at 1 amp. This is well within specification. However, the lot failed for beta max at I_C = 100. At this current level there is a beta window of 60 to 150. These devices read greater than 200. In general it was found difficult to home-in this device at emitter due to the relatively large beta and CEO. Recalculating the design, it was concluded that the epi thickness was on the shallow end. Specifications have been changed to increase the epi thickness by 2 microns. Meanwhile, another lot is running in the wafer area using the shallow epi thickness.

2N3960

Several confirmatory wafer lots have been started only to be rejected at emitter diffusion for either no base diffusion, shallow base diffusion,or no BV_{CBO} readings. These problems were finally analyzed as starting material variations. New material was ordered, started into processing, and is nearly finished. Sample probing indicated that all parameters were within specification.

2N4260

The confirmatory lot has been completed and is waiting for final test. Failure modes on previous lots (including one with 15 percent yield) were mainly V_{CE} (sat). The collector diffusion times have been increased from 20 to 60 minutes and sample probing confirmed that the V_{CE} (sat) specifications were easily met.

2N5115

The confirmatory lot was held for engineering prior to drain-source diffusion for tweaking. It was impossible to read the desired parameters due to the fact that some mask changes are required for process control. The lot was tweaked based on the I_{DSS} (V_G = 0) specification and was continued on for further processing. For future production controls it is imperative that a key or process control pattern be added to the mask set in the grid area to allow thickness limited breakdown to be measured prior to source-drain diffusion.

3.0 INTEGRATED CIRCUIT STATUS

3.1 PROCESSING STATUS

Work in the process area on the integrated circuits is proceeding satisfactorily. Five more confirmatory lots, in addition to the six confirmatory lots previously reported, have been circuit probed. Also, two first engineering sample lots, one second engineering sample lot, and five third engineering sample lots have been completed and circuit probed. Yields, in general, have been satisfactory, yet some lots have had low yields due to various reasons which will be explained in detail.

Results of the first, second, and third sample lots that have been completed are presented in Table II. Note that the 54LS193 circuit has not yielded well to date. The first lot, with zero yield, had resistor values that were double the value they should have been due to a malfunction of the ion implanter. This problem has since been corrected.

TABLE II

FIRST, SECOND, & THIRD SAMPLE LOTS
COMPLETED & PROBED

Date Probed	Device Number	Lot No.	Circuit Probe Yield %	No. of Good Die
9/15	5400	3	62.4	2,722
9/15	5401	3	63.6	1,943
9/15	5410	3	64.2	3,500
9/16	5473	3	51.6	1,796
10/16	54LS193	1	0	0
10/30	54LS194	1	20.0	861
11/12	54LS193	2	0.3	6
11/12	54LS193	3	5.2	97

The second and third lots of the 54LS193 device were processed together through most operations, except that lot 2 received a special "getter" step to improve breakdown voltages and possibly improve yields. As can be seen, the yield was reduced, not improved. It can also be seen that work is still needed to improve the "standard" yield on that part type.

Results of the confirmatory lots that have been completed and probed are given in Table III. Circuit probe yields are substantially above the goal of 26 percent with the exception of the 54LS138. The confirmatory lot of the 54LS138 device had several high yielding wafers (greater than 40 percent), yet the overall yield was 22.4 percent. The low yielding wafers are being analyzed to determine the predominant failure mode.

It is interesting to note that the second lot of the 54LS138 had a circuit probe yield of 49.7 percent, and lot 3 yielded 44.4 percent. Thus the yield potential is there.

TABLE III

CONFIRMATORY LOTS - COMPLETED & PROBED

Date Probed	Device Number	Circuit Probe Yield %	No. of Good Die
10/12	54LS74	39.4	2,130
11/11	5400	52.8	2,651
11/11	5401	39.7	1,688
11/11	5410	60.5	3,300
11/12	54LS138	22.4	1,001

Material that is being processed at the present time is now listed in Table IV.

TABLE IV

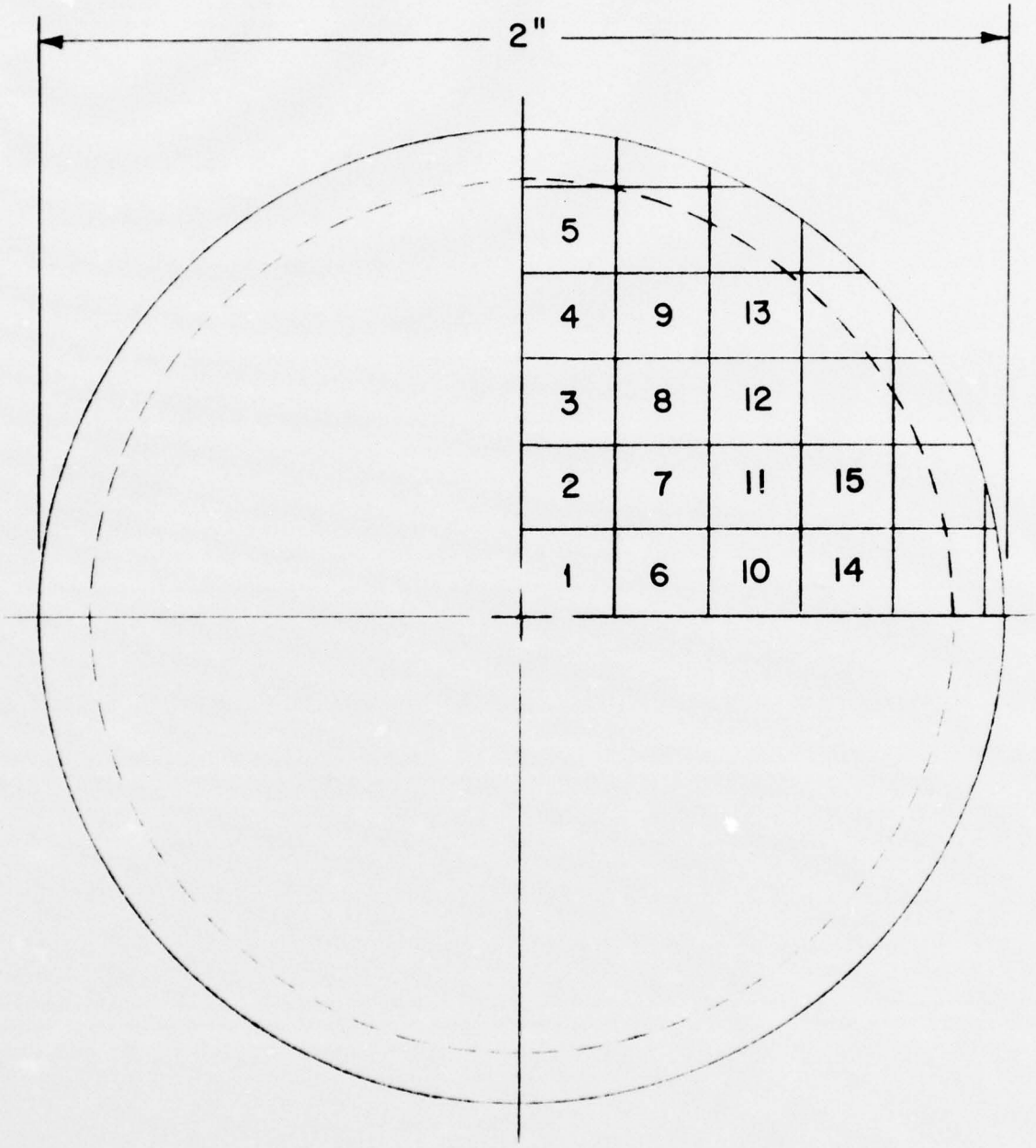
LOTS OF MATERIAL THAT ARE BEING PROCESSED

DEVICE NUMBER	LOT NUMBER	POSITION IN THE PROCESS
RA108	2	Emitter diffusion
RA108	3	Initial oxide
5473	Confirmatory	Sample probe
54LS194	2	Sealed junction oxide
54LS194	3	Sealed junction oxide
54LS73	Confirmatory	Starting material
54LS253	Confirmatory	Starting material

The work is progressing well on the above lots; no significant problems to date have been encountered.

3.1.1 Determination of the Number of Die on Each Wafer

In order to scientifically and accurately determine the number of die per wafer on the MM&T wafers, a computer program designed to count all die that are completely contained within a circle of a specified radius was written. See diagram in Figure 4.



EXAMPLE: 60 Die Per Wafer

Figure 4 WAFER YIELD DETERMINATION

The die in the outer 0.1 inch of the wafer were not counted, since that area has almost no potential for good die due to tweezer handling, photoresist build-up, mask scratching, etc. There is an occasional good die in this outer region; however, the yields are quite low even as far in as 0.2 - 0.3 inch from the edge of the wafer.

An outline of the computer program is now given:

```
      R =     Radius of wafer, excluding the 0.1 inch ring on the edge
      I =     Number of die
      X =     X dimension of the die, in mils.
      Y =     Y dimension of the die, in mils
      R =     900     (900 mil radius)
      I =     Ø
      X =     X Dim
      Y =     Y Dim
31    IF =    (SQRT ( ( X *X) + (Y * Y) ) -R) 5,10,10
      Y =     Y + Y Dim
      I =     I + 1
      Go to   31
10    IF =    (X-R 15, 20, 20)
15    X =     X + X Dim.
      Y =     Y Dim
      Go to   31
20    I =     4 * I   (I = Number of die)
      Return
      End
```

The results of the computer program are given in Table V.

TABLE V

COMPUTER CALCULATED DIE COUNT PER WAFER FOR MM&T DEVICES

DEVICE	DIE SIZE	NO. OF CENTER BLANKS, TEST & PROCESS CONTROL PATTERNS	POTENTIAL TOTAL NUMBER OF GOOD DIE
2N2907A, 2N2484, 1N3960 2N4260, 2N3251, 2N3639 2N5115, 1N746, 1N748	27 X 27	45	3327
2N3725, 2N3467, 2N3501 2N3635, 1N5314	36 X 36	20	1840
5400, 5401, 5410, 5440 54LS86	42 X 52	21	1079
5404, 5405, 54LS04, 54LS08, 54LS21, 54LS32, 54LS74	52 X 52	21	859
54LS73	52 X 62	21	707
54LS253	62 X 62	21	587
54LS138, 54LS194, 54LS196, 54LS197	62 X 72	21	503
5473	72 X 72	21	419
54LS193	82 X 92	9	287
RA108	102 X 145	9	135

All die on a 2.0 inch wafer are counted except:
1. Those that are 0.1 inch or less from the edge of the wafer.
2. Center blank die, test patterns, process control patterns.

3.2 DESIGN

3.2.1 Overview

The task of the Design and Layout Group during this quarter has been the completion of all final primary layouts with some additional effort on re-layouts and design corrections necessary to meet all specified parameters on the IC's. The RA108 metallization layout was submitted to the mask shop at the end of this quarter. Ten wafers of RA108 material have been processed up to preohmic and are on hold at that step. Once the metal masks are delivered, the wafers will be restarted into processing in order to meet the delivery date of December 20.

3.2.2 5400 Devices

Complete test data taken on packaged 5400 device types indicated that the input gate structure is marginal on meeting the input threshold voltage at temperature. The 5400 family is specified at 0.8 volt threshold, even at 125°C, while the 54LS family is specified at 0.7 volt. The same gate structure was used for both the 5400 and the 54LS parts. This is basically a high voltage structure, and Motorola had reason to believe that the input threshold voltage would be adequate for both types of circuits. This structure also offered speed advantages so it was adopted for 5400 use.

As the input is presently configured (shown as 54LS input gate in Figure 5), the threshold voltage goes up two VBE, up a Schottky, and down a VBE, so that:

$$Vt = 2\phi + \phi_S - \phi = \phi + \phi_S.$$

The input voltage thus equals a VBE plus a Schottky drop. At room temperature this becomes:

$$0.7V + 0.5V = 1.2 \text{ volts}.$$

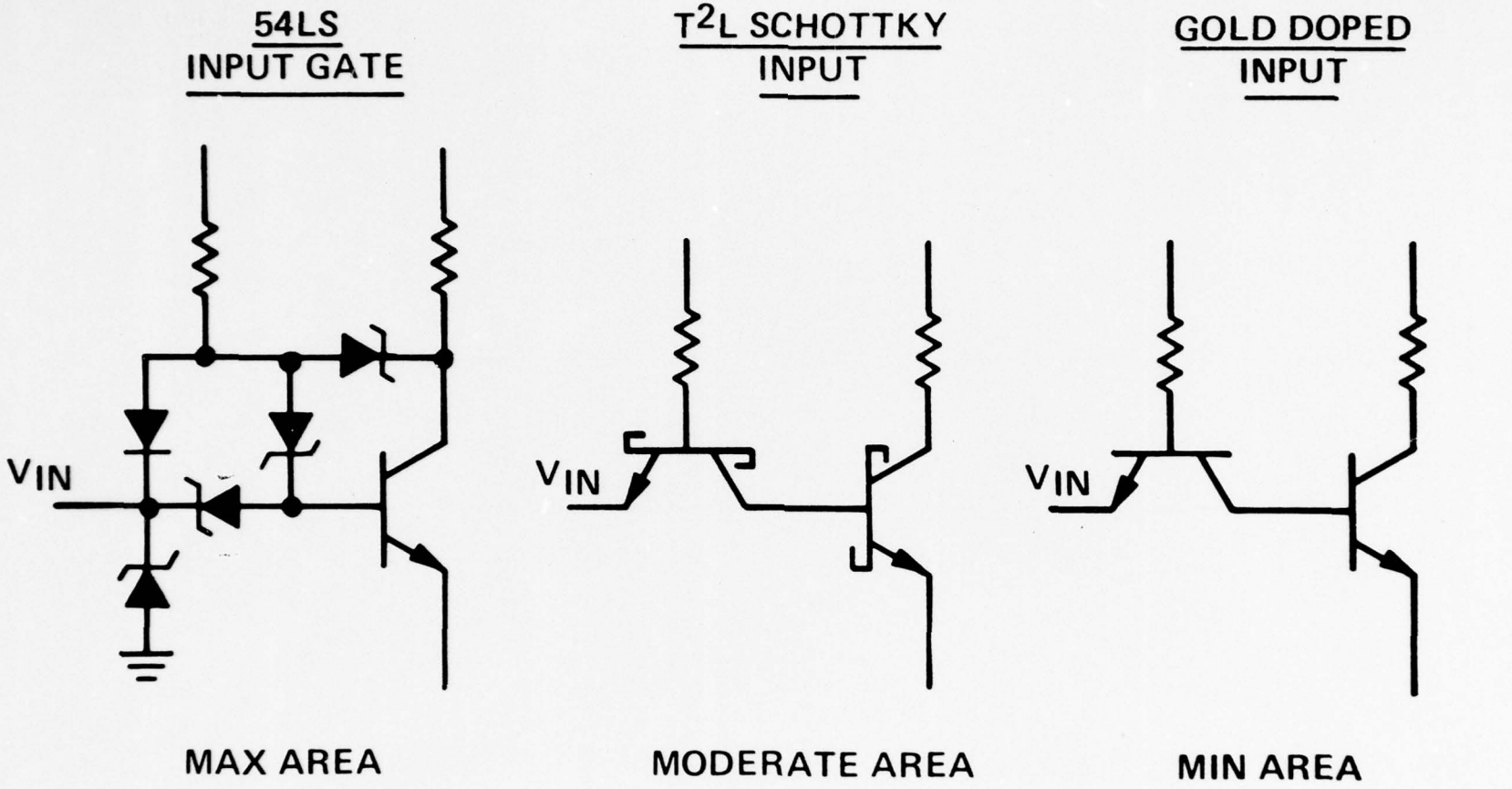


Figure 5. Input Gate Comparison

At high temperatures, however, this degrades to:

$$0.5V + 0.3V = 0.8 \text{ volt}$$

which is the spec limit. As a result there is severe yield loss to a 0.8 volt test spec, but a good yield to 0.7 volt.

One possible change presently being considered to correct this threshold problem is to substitute a Schottky diode for the PN diode. (This is accomplished, however, at the expense of 2 or 3 ns in turn-off speed, but this can be made up by a resistor correction.) The input threshold voltage thus becomes:

$$Vt = 2\phi + \phi_S - \phi_S = 2\phi$$

so the input voltage threshold now becomes simply 2 VBE. At room temperature this is:

$$2 \text{ VBE} = 2(0.7) = 1.4 \text{ volts.}$$

At high temperature (125°C) the input threshold voltage will become:

$$Vt = 0.5 + 0.5 = 1.0 \text{ volts @ } 125°C.$$

The input would now be 1.0 volt rather than 0.8 volt, or 200 mv higher, which will pass the 0.8 volt test spec. Redesign was completed on the 5473 dual JK to correct a toggle frequency problem. Devices will be available for testing in December.

3.2.2.1 Threshold Voltage Curves

The "Vin versus Vout" curves at different temperatures for the 5400 and 5404 part types are shown in Figures 6 and 7. These curves define the input threshold voltage that causes the output to change state from a "1" to a "zero." As can be seen, the room temperature and cold temperature curves exhibit ample threshold margin above the specified value. The high temperature curves approach the limit, sufficiently close that some yield loss due to marginal threshold voltage at high temperature is anticipated.

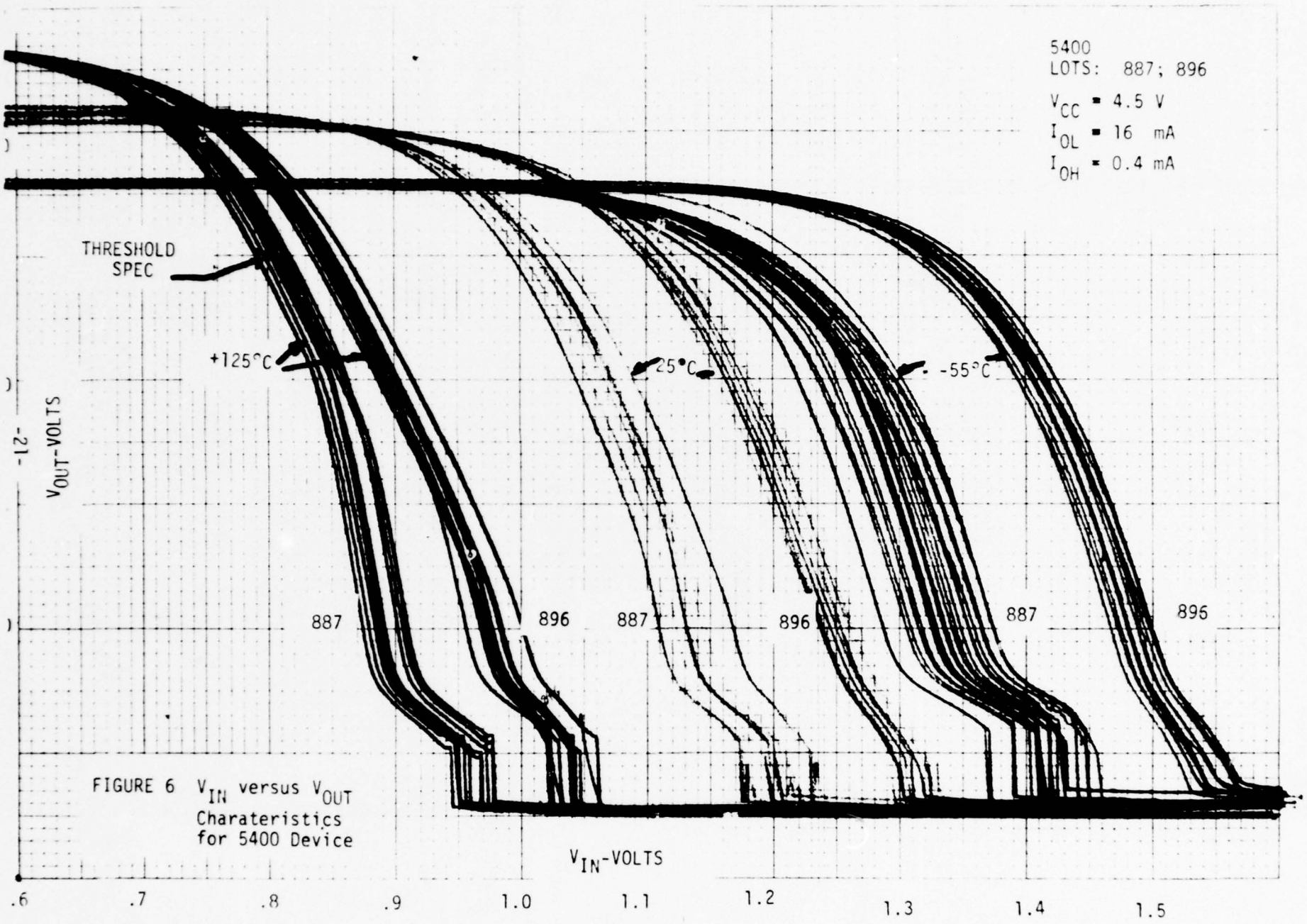


FIGURE 6 V_{IN} versus V_{OUT} Charateristics for 5400 Device

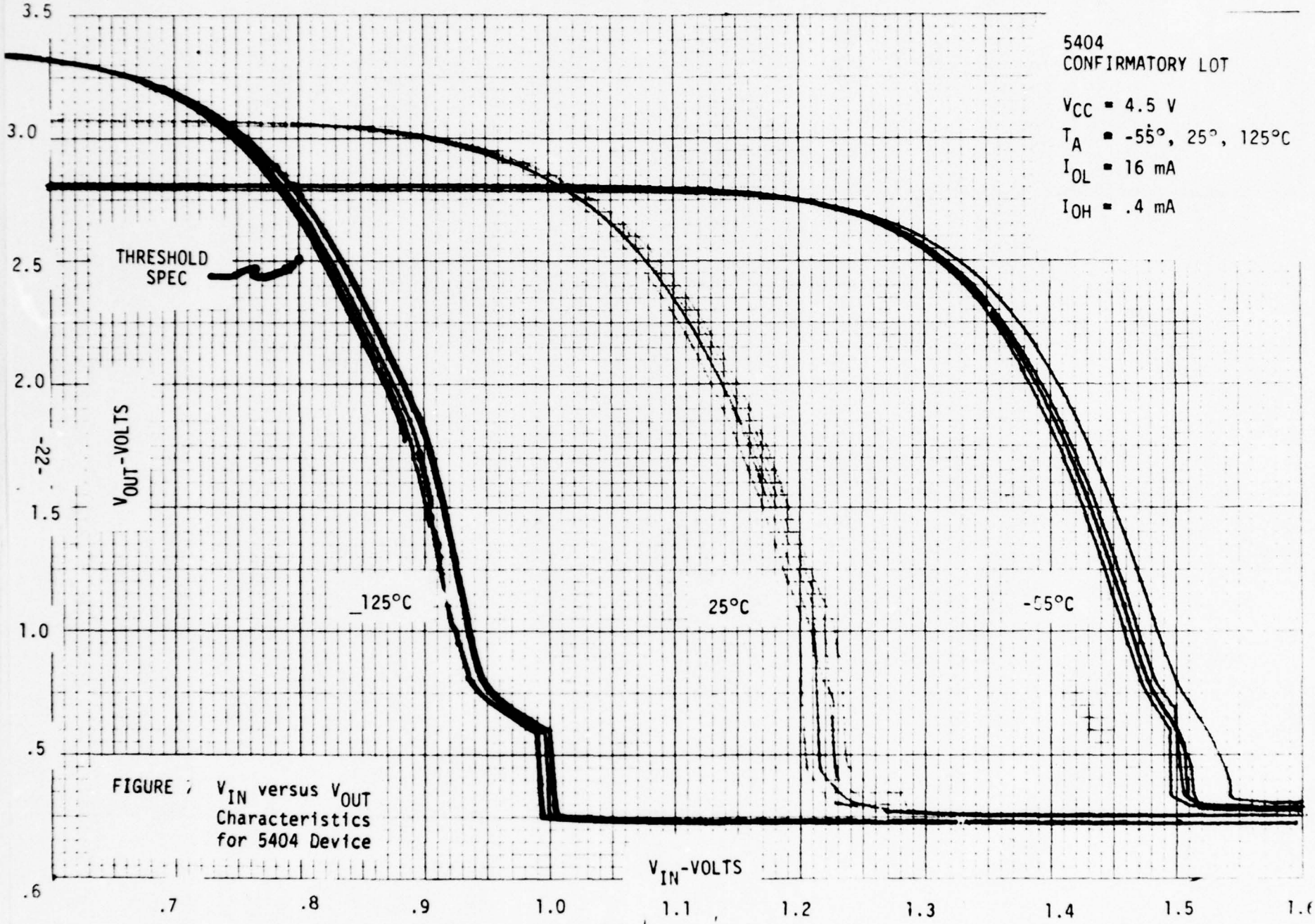


FIGURE 7 V_{IN} versus V_{OUT} Characteristics for 5404 Device

This yield problem could best be corrected with a mask change; however, yield may likely be improved through process control of desirable parameters.

3.2.3 54LS Devices

54LS196/7

This is the largest and most complex of the LS circuits in the program. Several layout attempts were required to achieve a layout compatible with the pre-determined chip size. This has been successfully done, but at a cost of many unique geometries not in the standard Calma device library. This will increase the Calma time required to digitize the circuit somewhat over the predicted time.

54LS73

Redesigns were completed on the LS73 to raise the toggle frequency and new masks are being fabricated.

54LS253

Design/layout improvements were implemented on the LS253 part during this past quarter. These have been completed and new starting material has been ordered. The success of these corrections will be evaluated by March.

4.0 PRODUCT ENGINEERING

At the completion of the design phase of this program it has been the intent of Motorola to transfer responsibility to the product engineering group for the confirmatory and pilot production phases.

Confirmatory is the phase of the program which requires establishing the manufacturing processes and methods that will be duplicated during pilot production.

It is recognized also that the increased quantity requirement of confirmatory and pilot production dictate a "systems" approach that was not necessary through the limited quantity phase of the design portion of the contract. This "systems" approach will also serve to satisfy the rate requirements of the contract (Section F.5, page 10).

To define the specific areas of control, the manufacturing area has been divided into five (5) groups:

1) Electrical specifications/slash sheets/qual tests
2) Internal electrical specs
3) Internal manufacturing document
4) Packages and package documentation
5) Burn-in boards.

With respect to these five areas, the various documents are being written to control all critical parameters and procedures for the two remaining phases.

4.1 SLASH SHEETS

Slash sheets have been requested on the following devices:

1N748	2N2484	2N3639	54LS21	5405
1N746	2N2907A	2N3960	54LS32	54LS04
1N5314	2N3464	54LS08	5404	

Additional specification requests have been held awaiting review of these initial documents. It was established that information gained from the critical analysis of a few specifications would make writing of the additional documents faster and easier. Documents covering the 1N746, 1N748 and 2N2484 have been released during this period.

4.2 INTERNAL ELECTRICAL SPECIFICATIONS

Emphasis has been placed on the generation of probe programs which will insert guardbands for temperature variations and possible test equipment tolerance variations. The temperature guardbands are based upon complete characterization of each device type at its temperature extremes (-55 and +125°C). Variations in the 25°C probe limits are then inserted to guarantee performance at temperature extremes.

Devices having completed all temperature testing are:

1N746	54LS08
1N748	54LS21
54LS04	54LS32

Typical values for various parameters on a 54LS type gate are shown along with a comparable shift for guardbands at probe.

PARAMETER	-55 - +125°C GUARANTEED LIMIT	25°C GUARDBANDED LIMIT
I_{IH}	20 µA	2 µA
I_I	100 µA	20 µA
I_{OS}	6-40 mA	9-37 mA
V_{OA}	2.5 V	2.7 V
V_{OL}	0.4 V	0.38 V
V_I	-1.5 V	-1.35 V

Recognizing that each device may have some variation to these values, it is still necessary to generate complete characterization of each device to insure reliable operation at extremes of temperature and voltage.

4.3 INTERNAL MANUFACTURING DOCUMENTS

The specifications for all areas of manufacturing have been initiated and various documents have been released in preparation of their use during pilot production. Documents already released include the three master flow specs which cover the wafer processing for all IC's plus control of all contract requirements for both discrete and IC devices.

Also currently under review are the front and backside visual inspections. Upon approval of these documents the only remaining document will be the assembly shop order. Once this is approved we are then fully within the current manufacturing system and can expand to meet quantities.

4.4 PACKAGES AND PACKAGE DOCUMENTATION

Packages for confirmatory testing have been ordered. The specification covering the bonding of these chips in packages is currently under review and will be released as needed.

4.5 BURN-IN BOARDS

Burn-in boards have been designed and are currently under construction. All schematics have been approved and all components have been ordered. Delivery times are adequate to meet the program schedule.

5.0 PACKAGING

5.1 INTRODUCTION

It was explained in previous contract reviews that packages for the beam lead integrated circuits were not available; therefore, either packages or chip carriers had to be designed and developed for this program. Once the decision was made by the Army in August not to fund a development program for the chip carriers, design of the packages for the IC's was initiated.

5.2 INTEGRATED CIRCUIT PACKAGES

Appendix A includes the manufacturing assembly drawings required in fabricating the packages for the twenty 5400 and 54LS IC's. An explanation of these drawings follows:

1. Sheet one (1) of drawings 18CSM21009A and 18CSM21015A is the general concept of the final assembly for those devices listed.

2. Sheet two (2) of these same drawing numbers delineates the dimensional requirements for the lead frames in relation to the ceramic, again for those same devices listed on Sheet 1.

3. Sheet three (3) provides the basic metallization, dimensions, and critical tolerances for these same devices.

4. The remaining sheets in each of these two sets of drawings depict the beam-to-pin-out relationshp for each individual device as shown on the metallization patterns.

5.3 RA 108 60 GATE ARRAY

The package for this large chip is still being designed. For the purpose of testing the second and third engineering samples, substrates have been ordered from an outside vendor.

5.4 DISCRETE PACKAGES

The TO-5 and TO-18 packages required for all of the discretes were designed by Motorola several years ago. Because of age, new tooling was ordered and packages are scheduled to be delivered by the end of December.

6.0 CONCLUSIONS AND PLANS FOR NEXT QUARTER

6.1 CONCLUSIONS

It has been demonstrated that both the 5400 and the 54LS processes have been established and are well under control. Such is not the case for the discrete devices, as clearly shown in Section 2.0. Although the various processes for each of the discretes have or soon will be established, precise control as required under this contract may not be possible. This does not mean that they cannot be fabricated, but to consistently achieve a probe yield of 48 percent for a specific device may be impractical. This probe yield is what is believed to be the lower limit in order to achieve the overall contract yield goal of 20 percent.

6.2 PLANS FOR NEXT QUARTER

6.2.1 Discrete Devices

Additional lots of each discrete device type will be processed in order to improve the yields, but only minor changes will be made since most of the processes, as stated previously, have or soon will be established.

6.2.2 Integrated Circuits

Some of the integrated circuits will be submitted to qualification testing during the next three months. Others, such as the LS04, LS08, and LS32 will be completely characterized over temperature. Any design problems will be recognized at that time. First samples will be available for testing on the RA108.

6.2.3 Packages

The packages have been designed with exception of the RA108, as outlined in Appendix A, and sufficient quantities of all required types will be available for the confirmatory qualification test program. Design will be completed on the RA108 package during the next quarter.

APPENDIX A

BEAM LEAD DEVICE PACKAGES

LTR	REVISIONS
0	IC-0480610 RELEASED FOR PRODUCTION ECO 10-20-76

NOTES

1.0 STANDARD NOTE SPECIFICATION 00ASM21017A IS PART OF THIS DRAWING AND THE REQUIREMENTS SPECIFIED THEREIN SHALL APPLY TO PARTS MANUFACTURED PER THIS DRAWING.

2.0 FLAG INDICATES LEAD NUMBER -1.

3.0 NUMBERS SHOWN ARE FOR REFERENCE ONLY AND SHALL NOT APPEAR ON THE PART.

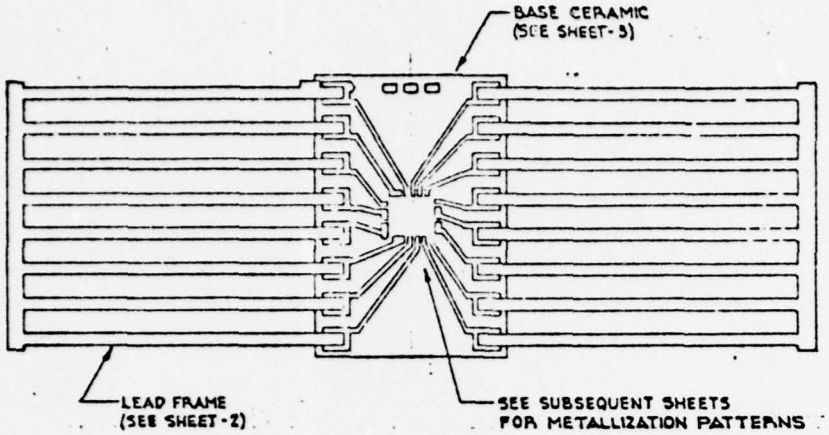
4.0 APPLICABLE DEVICE NUMBER INDICATED SHALL BE LEGIBLE WITHOUT MAGNIFICATION ON EACH PART.

5.0 SPACE BETWEEN ADJACENT METALLIZATION WITHIN THE .010 MIN ZONE SHALL BE .001 MIN.

6.0 PROFILE TOLERANCE SHALL BE HELD WITHIN THE .010 MIN ZONE.

7.0 BEAM BOND PADS IN THE .010 ZONE SHALL BE FLAT WITHIN .0002.

8.0 PACKAGE AND MARK PER 12ASM21034A.



18CSM21009A

18CSM21009A004	LEAD FRAME ASSY (FOR DEVICE MT-54LS253)
18CSM21009A003	LEAD FRAME ASSY (FOR DEVICE MT-54LS194)
18CSM21009A002	LEAD FRAME ASSY (FOR DEVICE MT-54LS189)
18CSM21009A001	LEAD FRAME ASSY (FOR DEVICE MT-54LS138)
MOTOROLA PART NO.	DESCRIPTION

DIM. & TOL. PER ANSI Y14.5 1973

DUAL DIMENSIONING REFERENCED THUS [illegible] INCH CONTROLLING DIMENSION INCH

THIRD ANGLE PROJECTION

CASE NO.

SERIES

TOLERANCE UNLESS NOTED: FRACTIONS ±; INCHES; PLACES ± ; PLACES ±

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STD NOTES	00ASM21017A
BILL OF MATERIAL	01ASM21082A
ORIGINATOR	D. DIDDAMS
DATE	7-26-76
DRAWN BY	K. B. SMITH
DATE	11-7-72
CHECKED BY	[illegible]
DATE	[illegible]

SIZE C

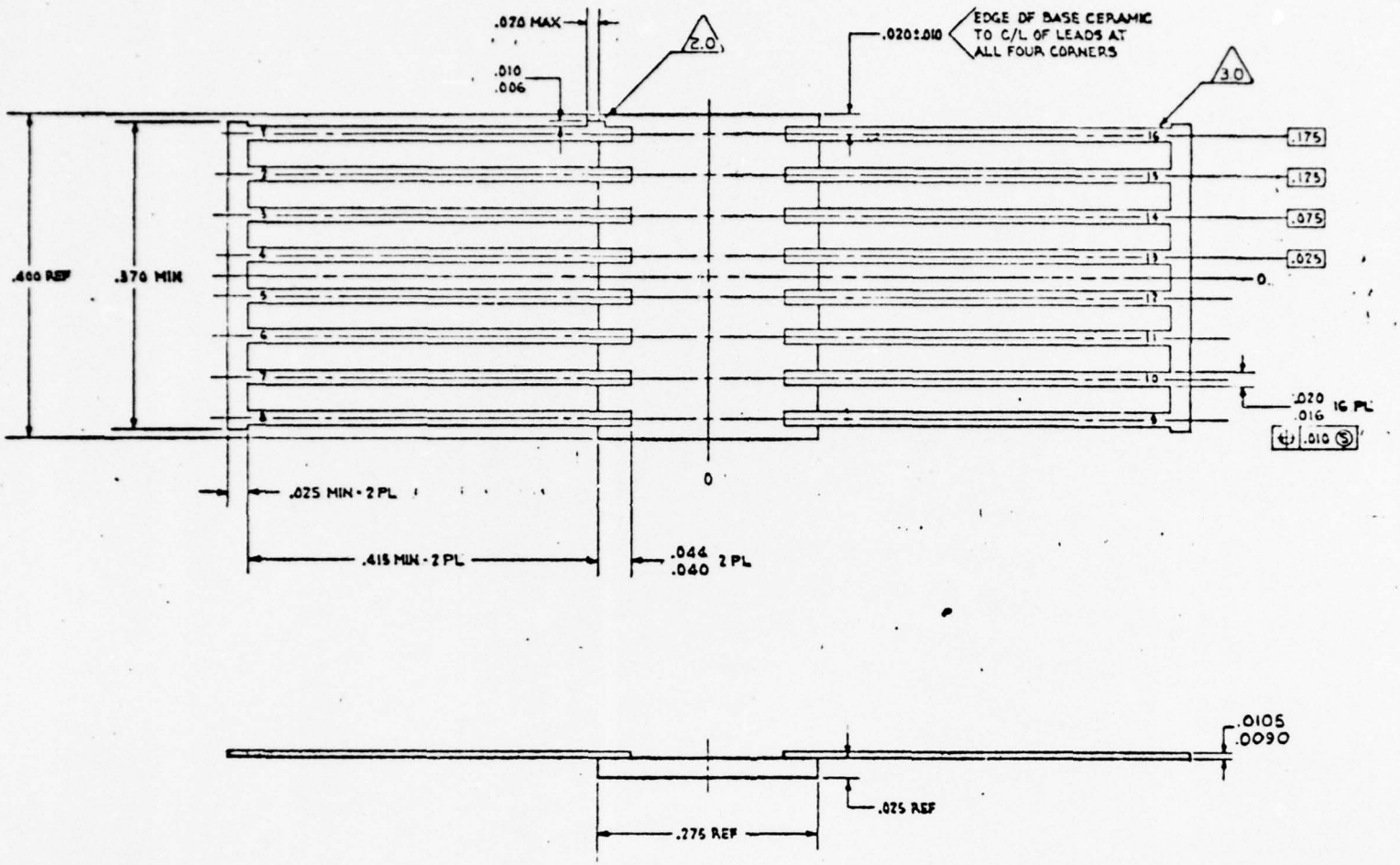
MOTOROLA INC. Integrated Circuits Division

TITLE: LEAD FRAME ASSY, BEAM LEAD (16 LEADS) (MM&T)

PROD GROUP: FEDERAL MIREL

18CSM21009A

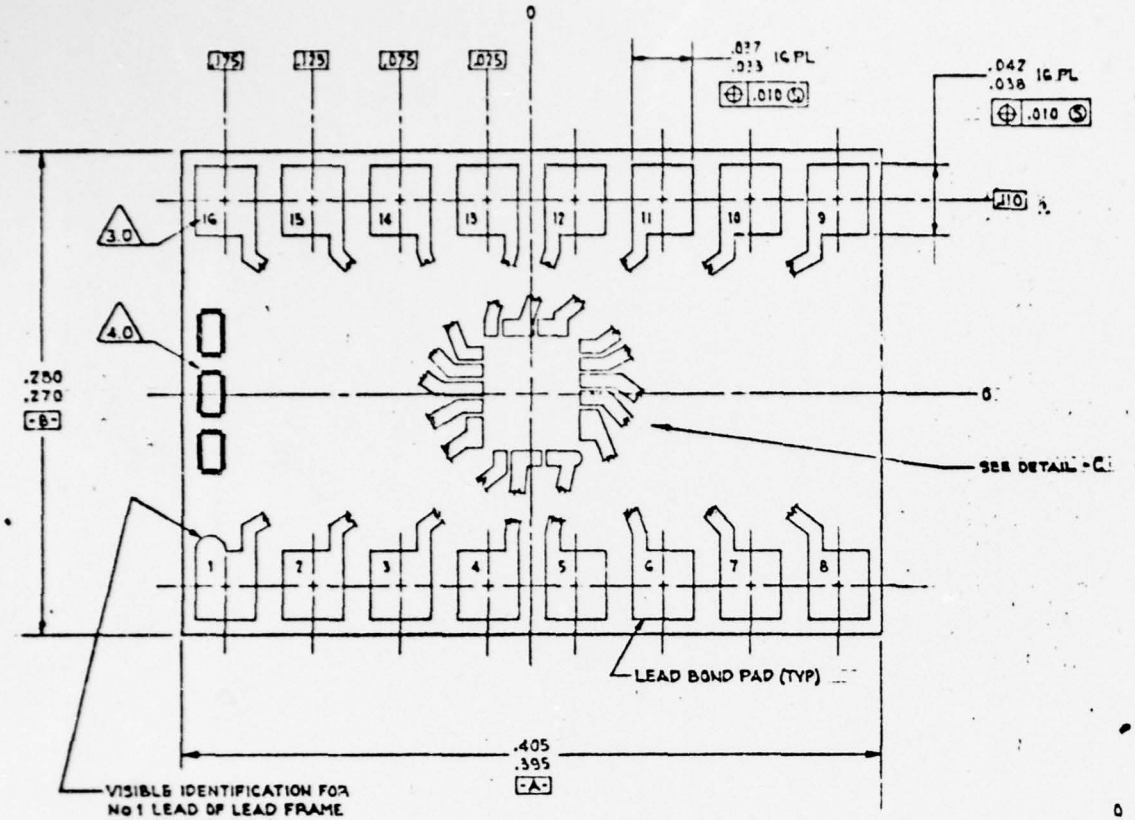
CODE (MFG): [illegible] SCALE: [illegible] SHEET 1 OF 2



LEAD FRAME (16 LEADS)

SCALE • 10/1

SIZE C | DWG NO 18CSM21009A | REV LTR D | SHEET 2 OF 7



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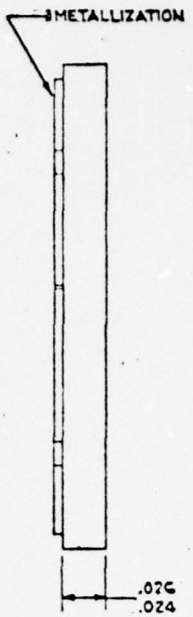
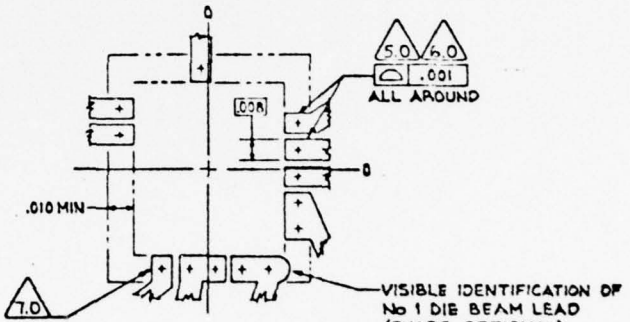
SCALE = 20/1





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BEAM BOND AREA

SEE CONTINUATION SHEETS FOR PATTERNS

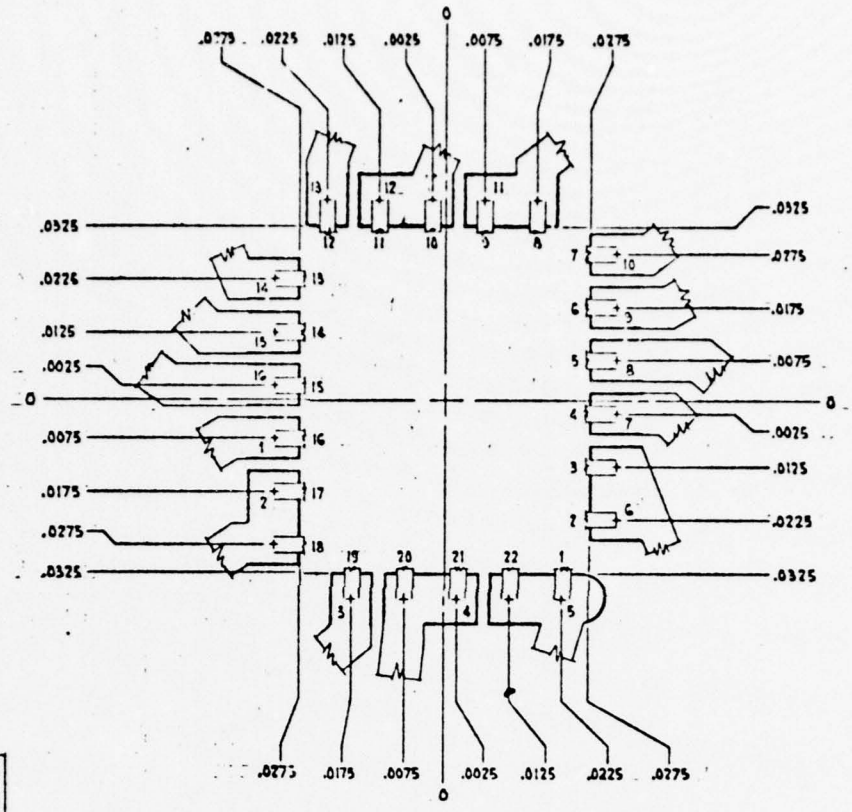
18CSM21009A

SIZE C

DWG NO 18CSM21009A

REV LTR 0

SHEET 3 OF 7

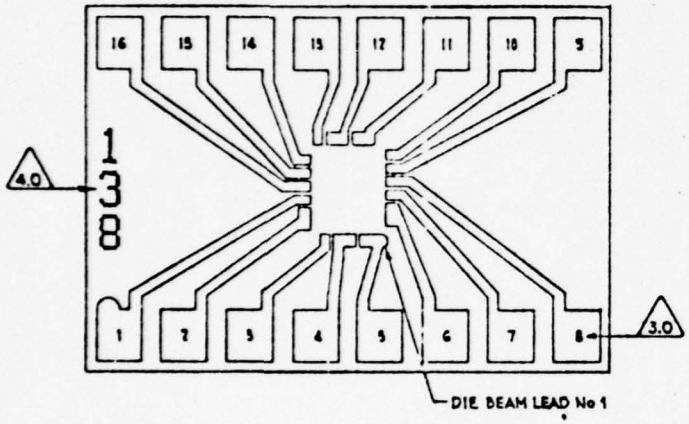


BEAM BOND PADS

ALL DIMENSIONS ARE BASIC

SCALE 60/1

18CSM21009A



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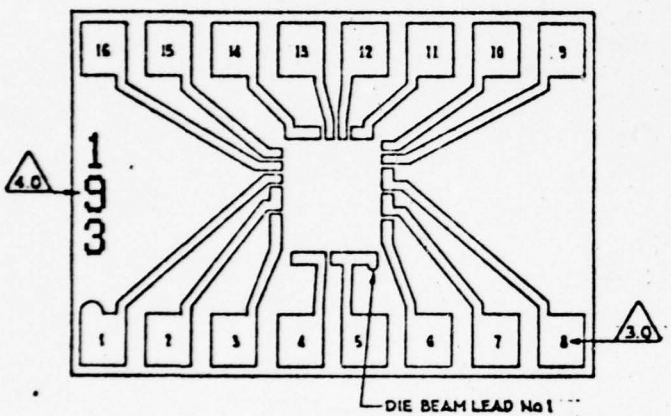
SHEET 8 OF 7



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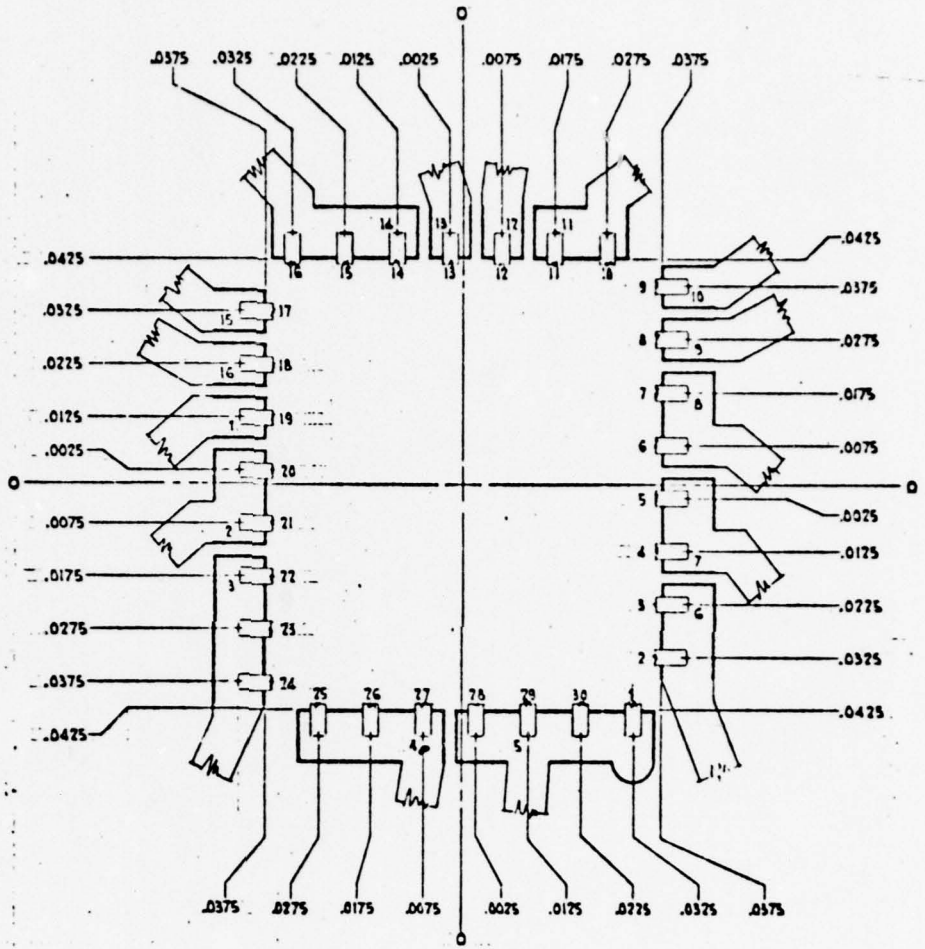

BEAM BOND PADS

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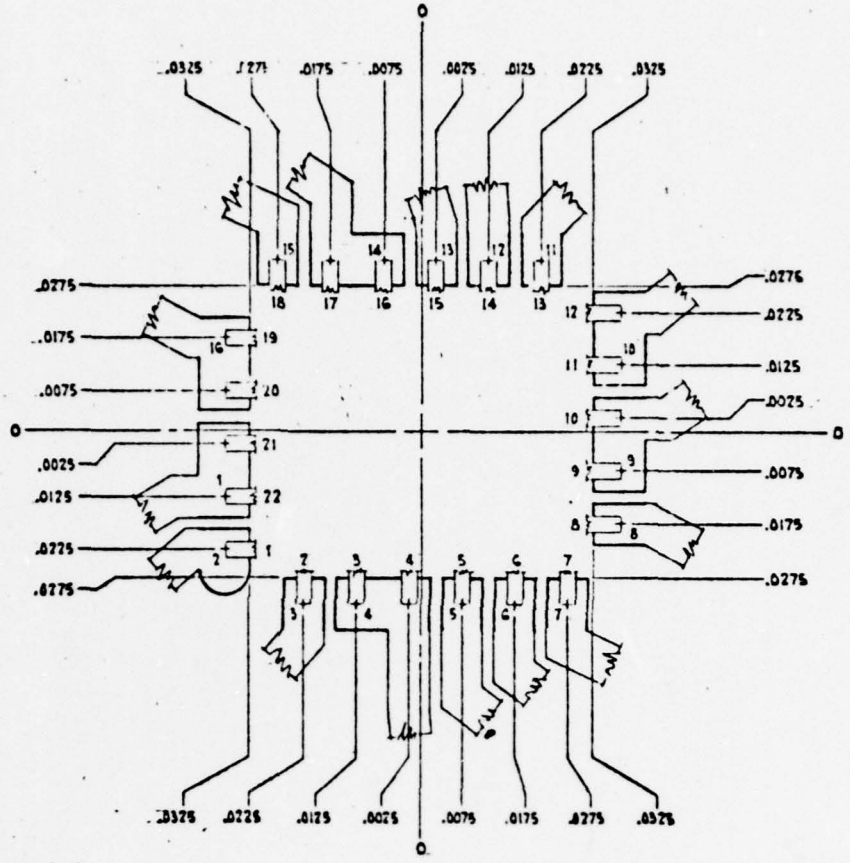
SCALE 60/1

PART No A002

18CSM21009A

C 18CSM21009A



BEAM BOND PADS

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SCALE 60/1

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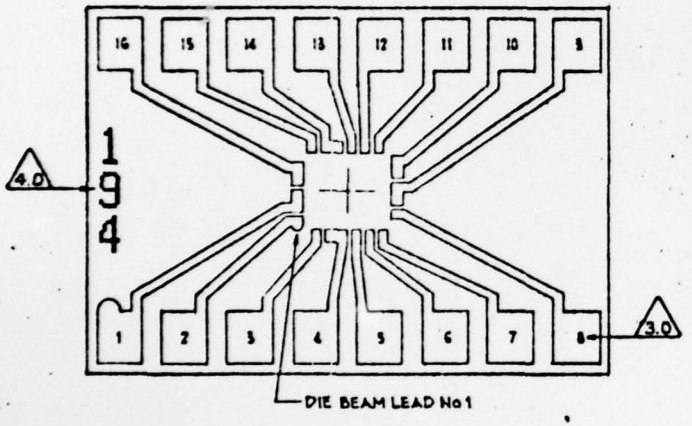

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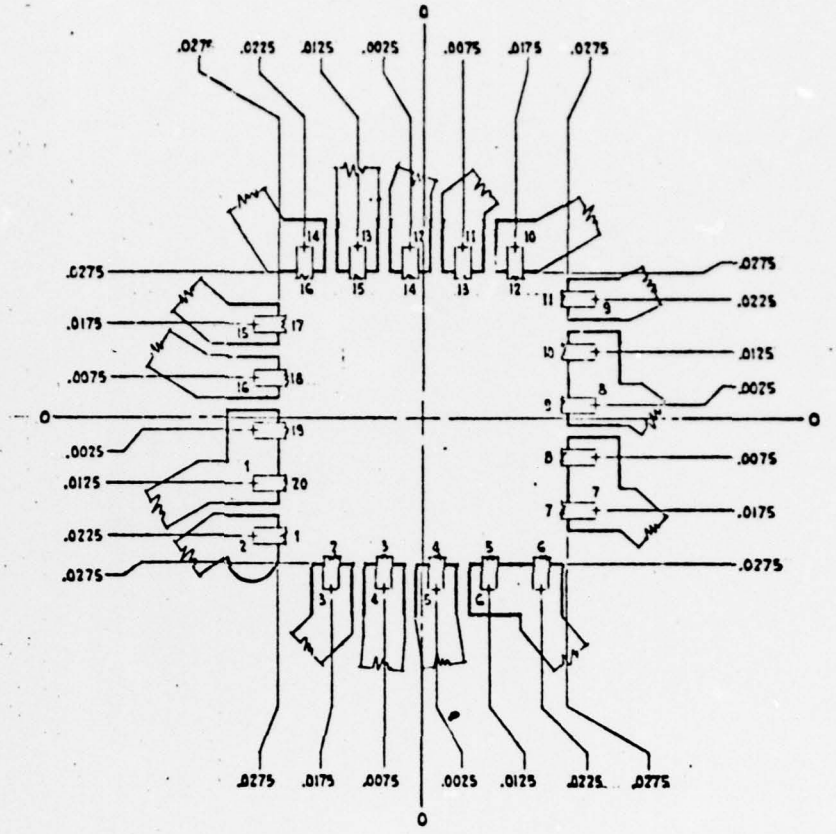

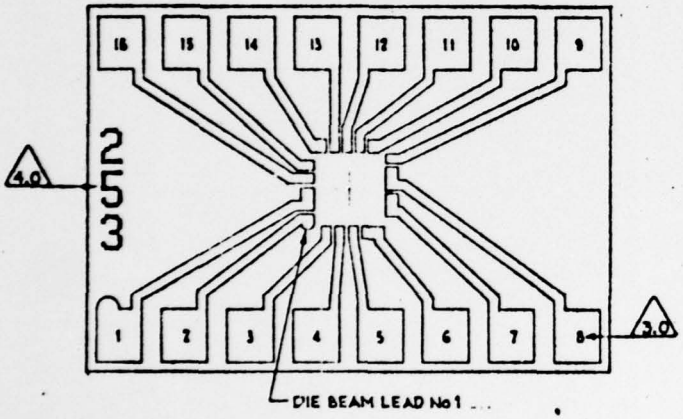

METALLIZATION PATTERN

BEAM BOND PADS

ALL DIMENSIONS ARE BASIC
SCALE 60/1

PART No A004

18CSM21009A

SIZE	DWG NO	REV
C	18CSM21009A	0

SHEET 7 OF 7

LTR	REVISION
0	IC-0512610 REL FOR PRODUCTION JED 10-20-76

NOTES

1.0 STANDARD NOTE SPECIFICATION 00ASM21017A IS PART OF THIS DRAWING AND THE REQUIREMENTS SPECIFIED THEREIN SHALL APPLY TO PARTS MANUFACTURED PER THIS DRAWING.

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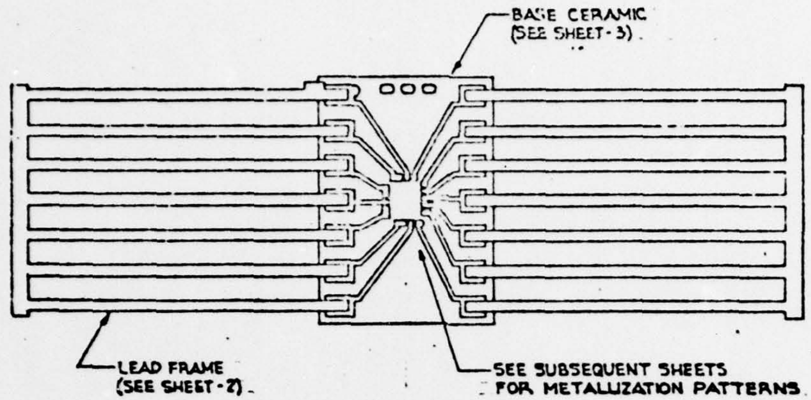
6.0 PROFILE TOLERANCE SHALL BE HELD WITHIN THE .010 MIN ZONE.

7.0 BEAM BOND PADS IN THE .010 ZONE SHALL BE FLAT WITHIN .0002.

8.0 PACKAGE AND MARK PER 12ASM21035A.



18CSM21015A

BEST AVAILABLE COPY

MOTOROLA PART NO.	DESCRIPTION
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A009	(REF. DEVICE MT-54LS76)
A008	(REF. DEVICE MT-5473)
A007	(REF. DEVICE MT-5400, -5401) (REF. DEVICE MT-5410, -5440)
A006	(REF. DEVICE MT-5404, -5405)
A005	(REF. DEVICE MT-54LS04)
A004	(REF. DEVICE MT-54LS32)
A003	(REF. DEVICE MT-54LS08) (REF. DEVICE MT-54LS21)
A002	(REF. DEVICE MT-54LS196, -54LS197)
18CSM21015 A001	LEAD FRAME ASSY (REF. DEVICE MT-54LS73)

DIM & TOL PER ANSI Y14.5 1973

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DUAL DIMENSIONS DEPICTED THUS
CONTROLLING DIMENSION: INCH
THIRD ANGLE PROJECTION

CASE NO
SERIES

TOLERANCE UNLESS NOTED — INCHES
PLACES 1 — PLACES 2 —

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STD NOTES	00ASM21017A	
BILL OF MATERIAL	01ASM21081A	
ORIGINATOR	D.DIDDAMS	DATE 7-26-76
DRAWN BY	K.R.SMITH	DATE 8-31-76
CHECKED BY	[illegible]	DATE [illegible]

SIZE C

MOTOROLA INC.
Integrated Circuits Division

TITLE: LEAD FRAME ASSY BEAM LEAD (14 LEADS) [MM4T]

PROD GROUP: FEDERAL HI REL

DWG NO. 18CSM21015A

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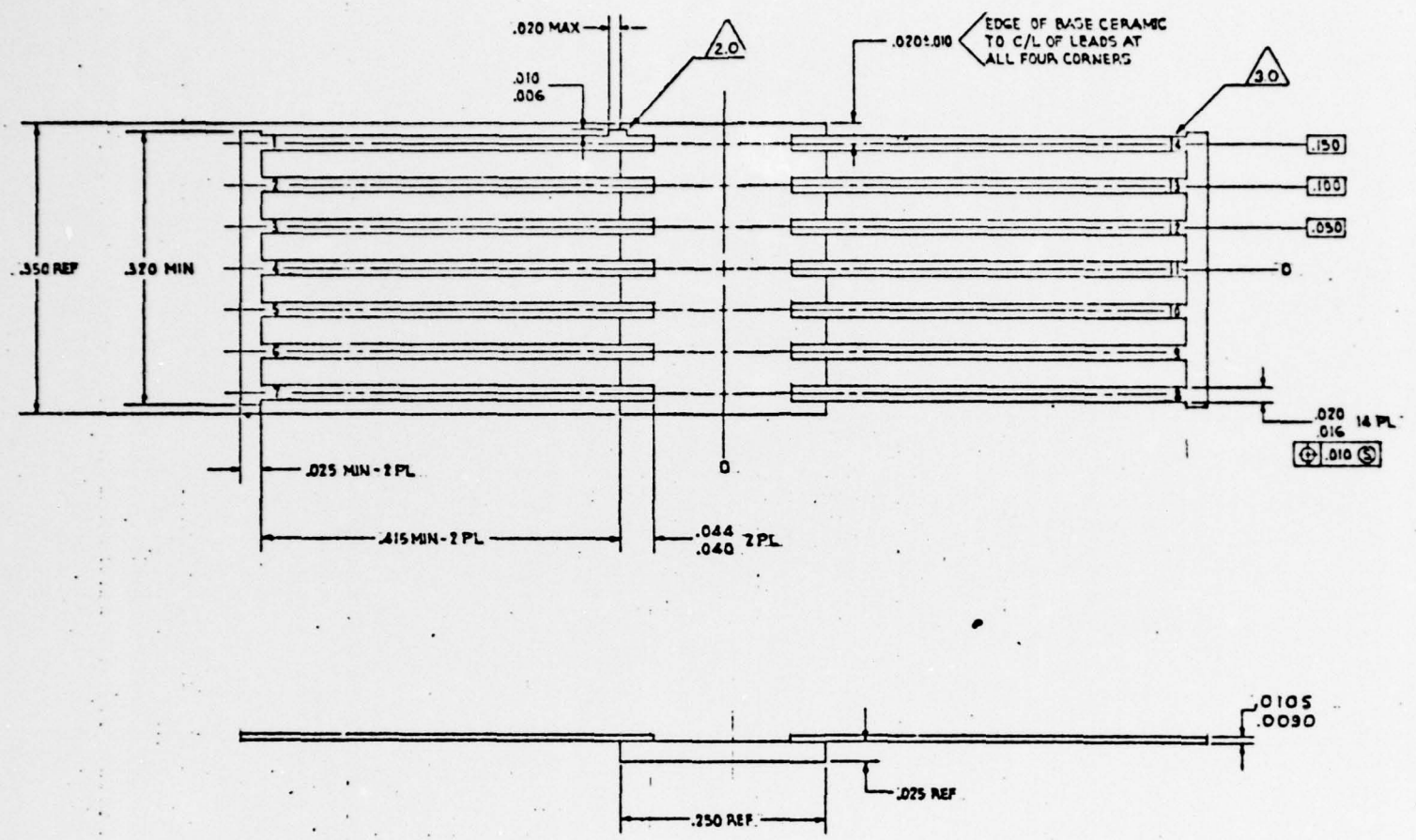

18CSM21015 A

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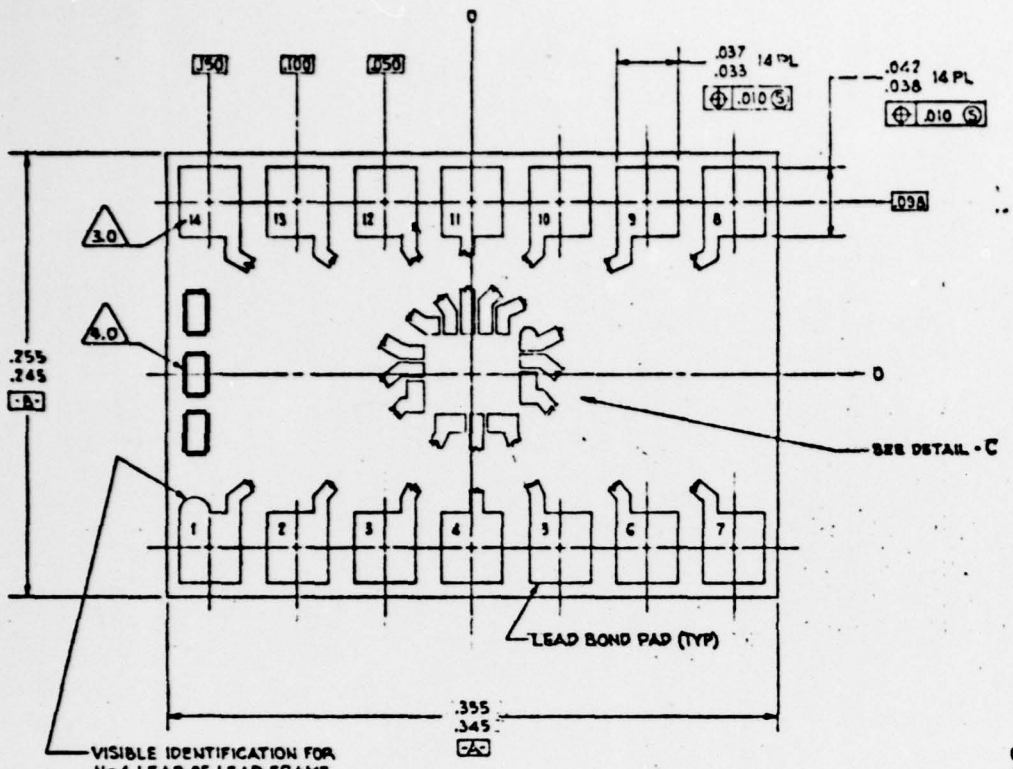

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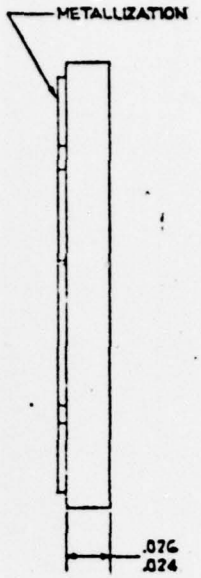

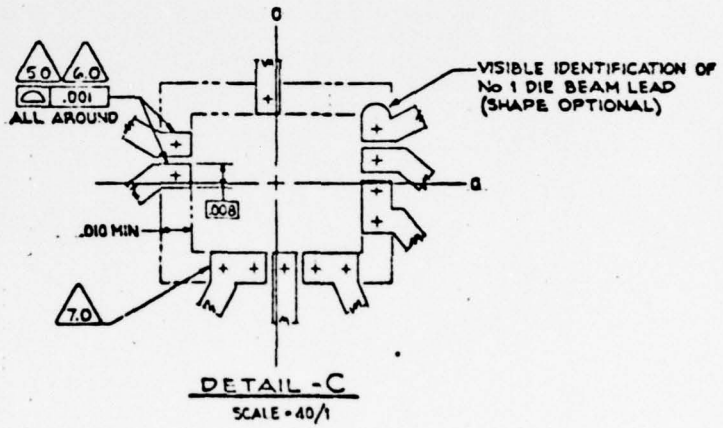

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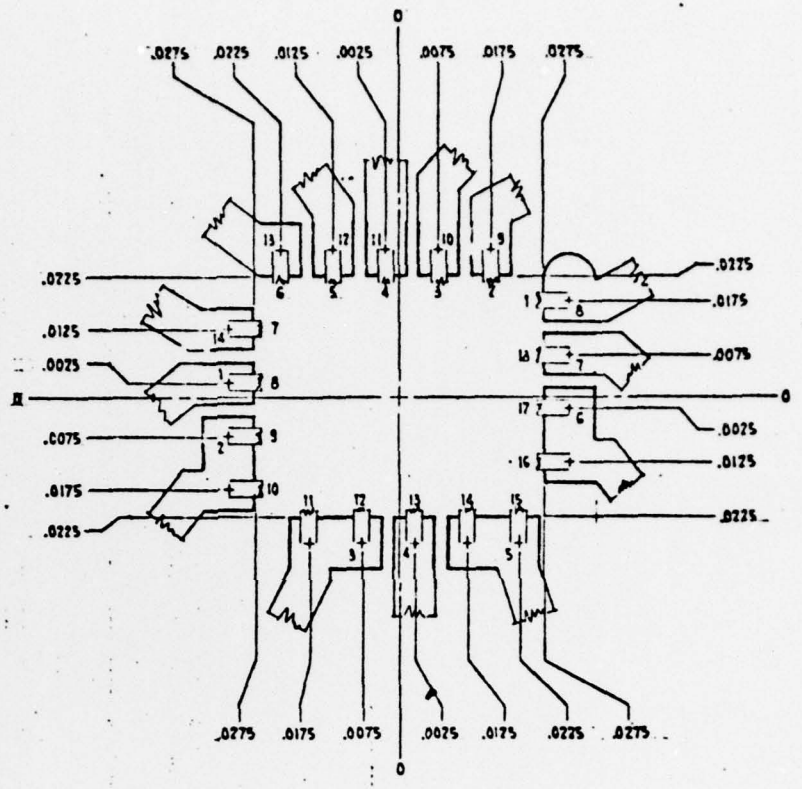
BEAM BOND AREA

SEE CONTINUATION SHEETS FOR PATTERNS

18CSM21015 A

SIZE C | 18CSM21015 A

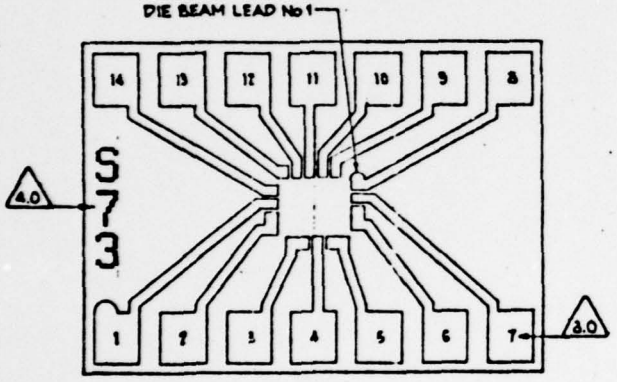


BEAM BOND PADS

ALL DIMENSIONS ARE BASIC

SCALE 60/1

18CSM21015 A



METALLIZATION PATTERN.

PART No A001

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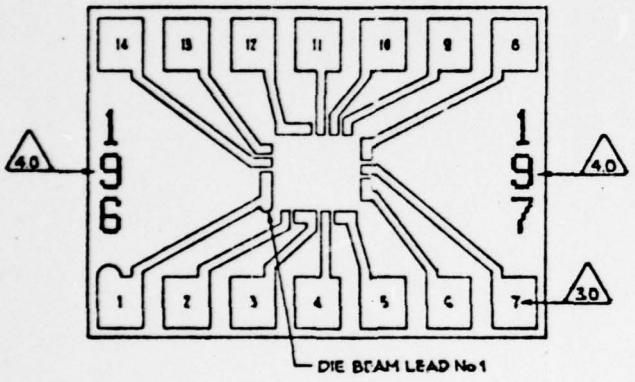
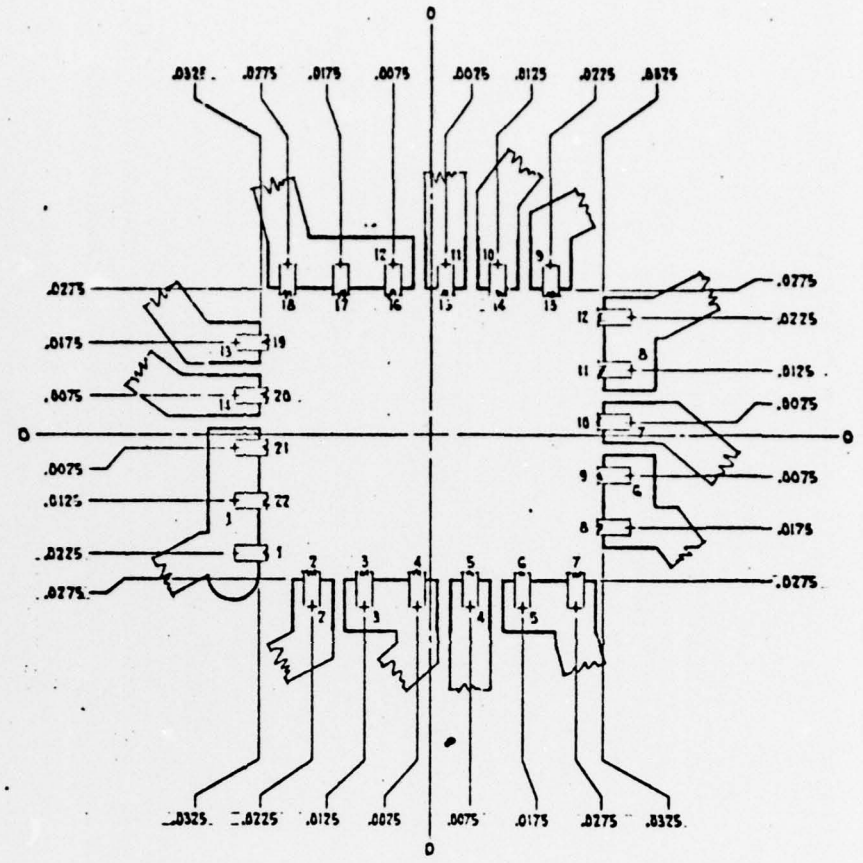


METALLIZATION PATTERN



BEAM BOND PADS

ALL DIMENSIONS ARE BASIC.
SCALE 60/1

PART No A002

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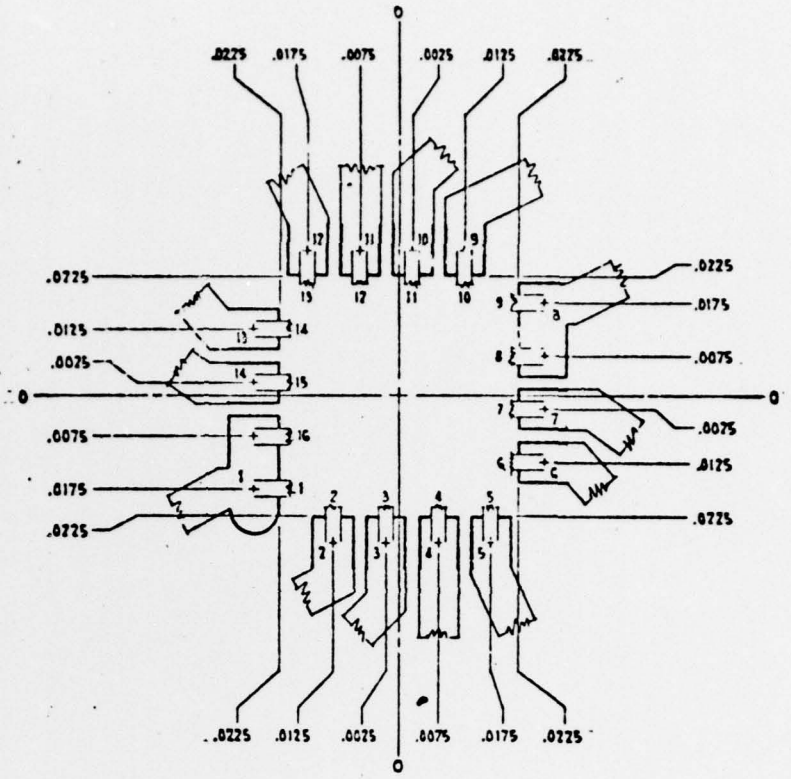

BEAM BOND PADS

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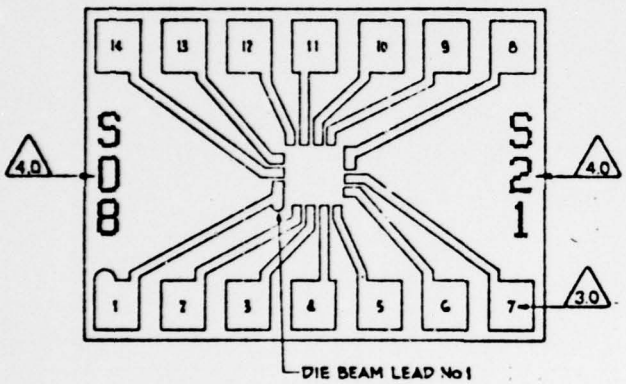
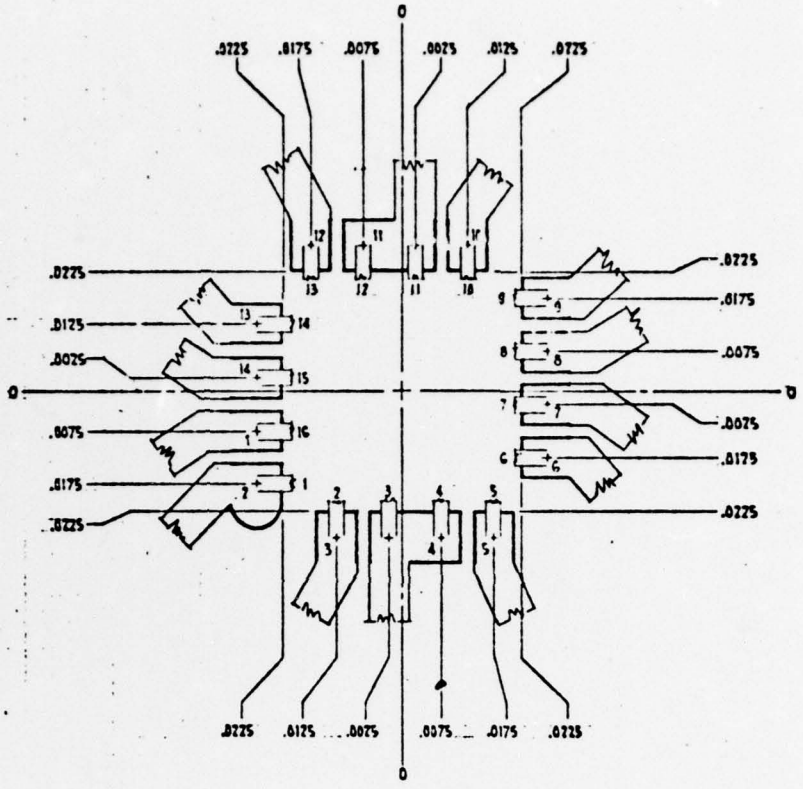


METALLIZATION PATTERN

PART No A 003

18CSM21015 A

SIZE C | 18CSM21015 A



BEAM BOND PADS

ALL DIMENSIONS ARE BASIC

SCALE 60/1

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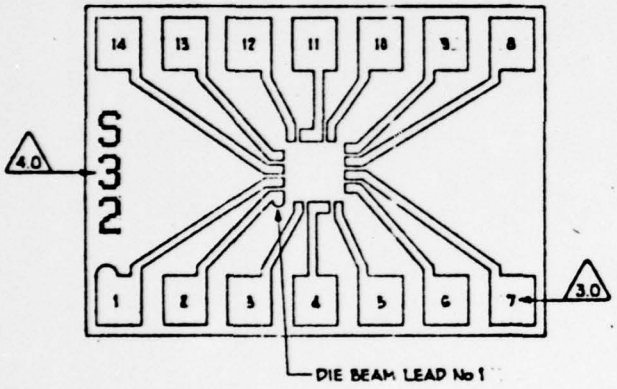
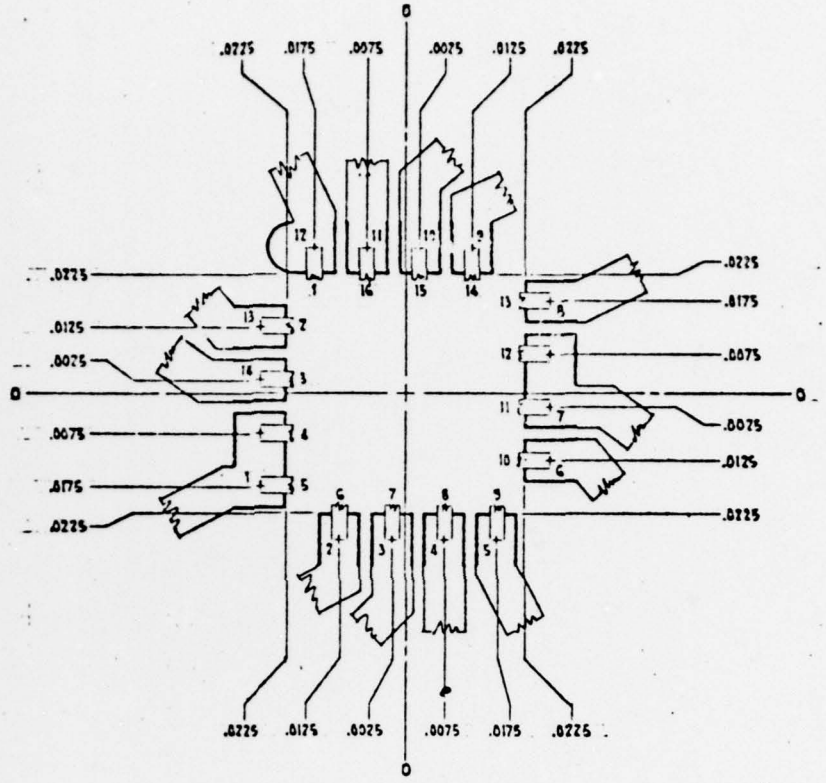


METALLIZATION PATTERN

18CSM21015 A

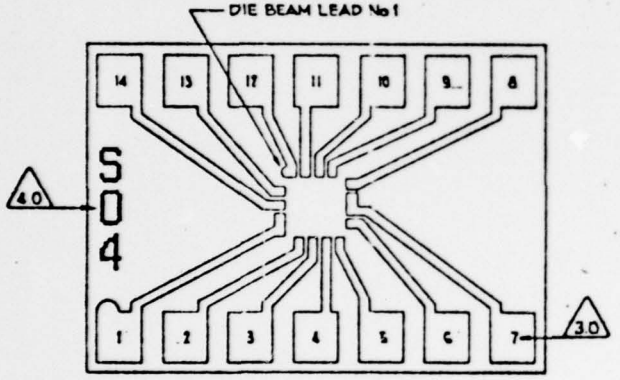
SIZE C | DWG NO 18CSM21015 A | REV LTR O | SHEET 2 of 3



BEAM BOND PADS

ALL DIMENSIONS ARE BASIC

SCALE 60/1



METALLIZATION PATTERN

PART No A005

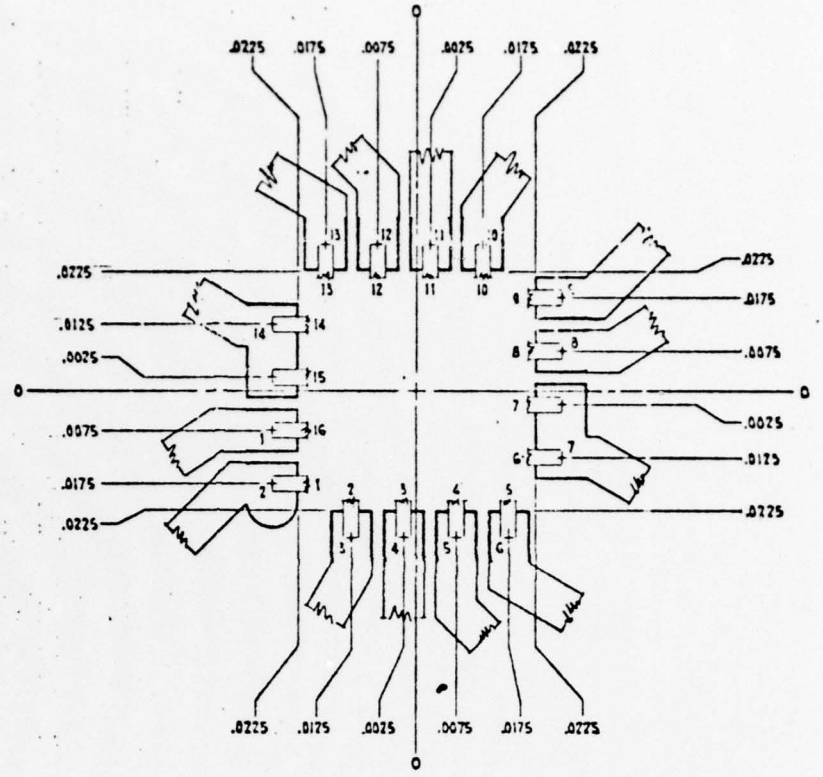
18CSM21015 A

SIZE C

DWG NO 18CSM21015 A

REV LTR O

SHEET 2 OF 3

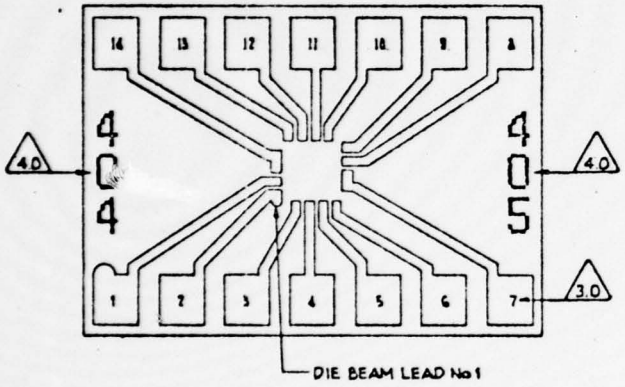


BEAM BOND PADS

ALL DIMENSIONS ARE BASIC

SCALE 60/1

PART No A006

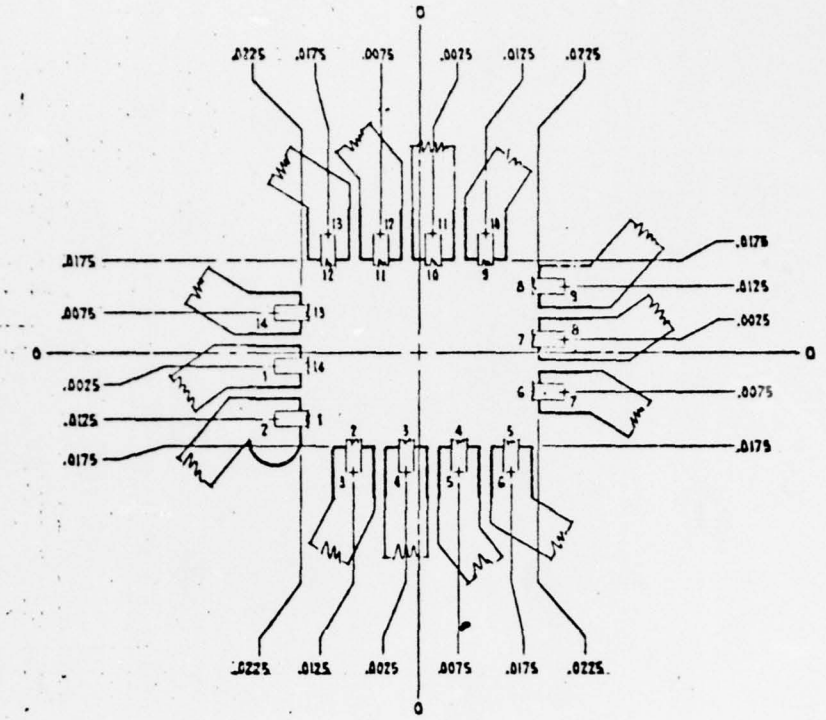


METALLIZATION PATTERN

18CSM21015 A

SIZE	CAGE NO	18CSM21015 A	REV LTR
C			C

FOR REVISIONS SEE SHEET 1

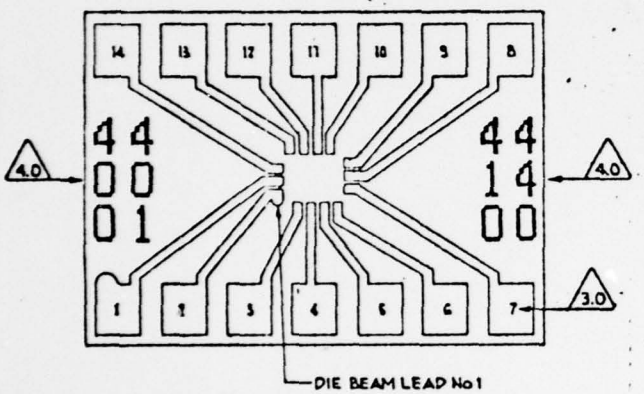


BEAM BOND PADS

ALL DIMENSIONS ARE BASIC

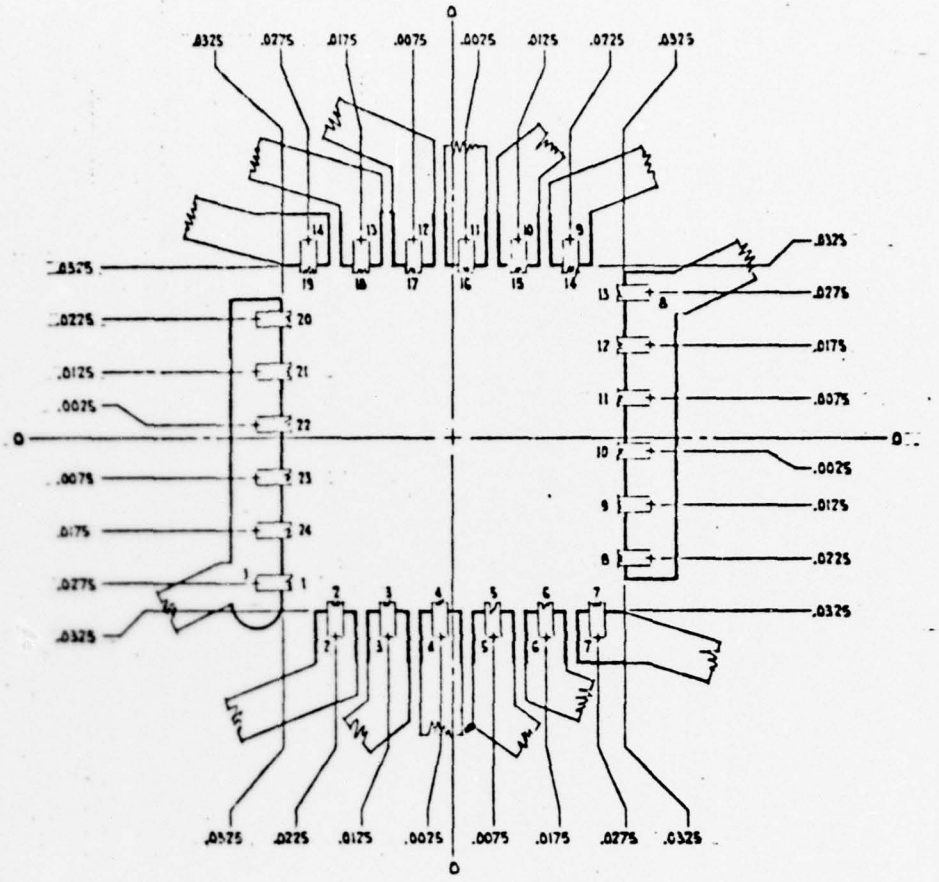
SCALE 60/1

PART No A007



METALLIZATION PATTERN

DWG NO 18CSM2101SA

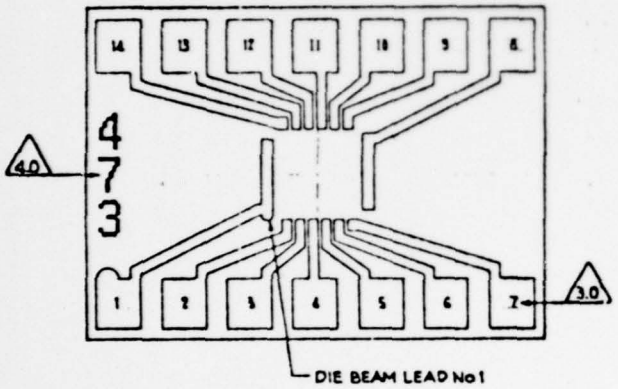


BEAM BOND PADS

ALL DIMENSIONS ARE BASIC

SCALE 60/1

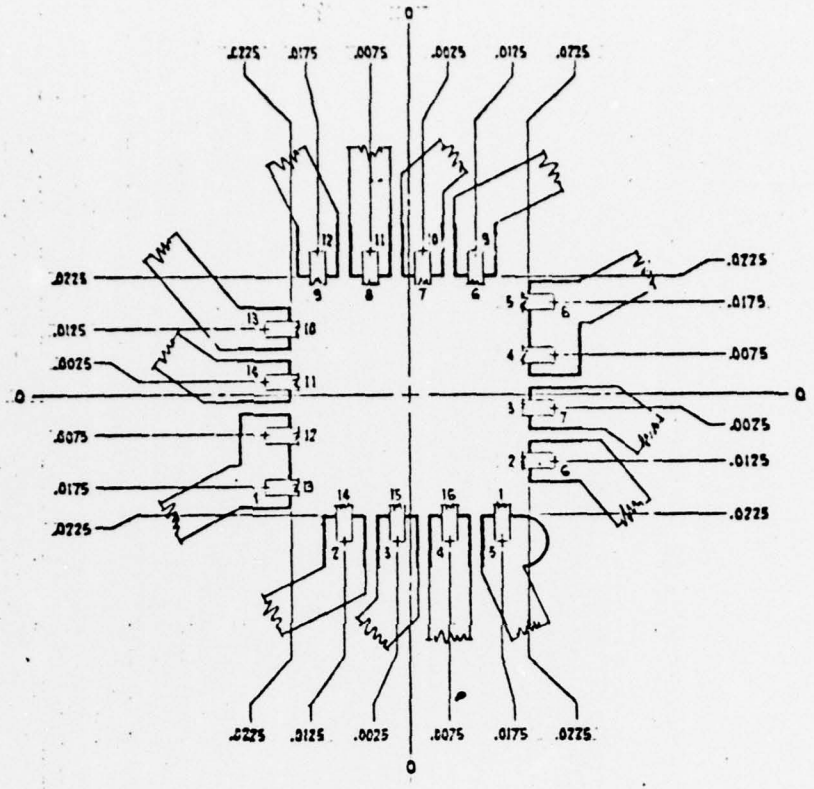
PART No A008



METALLIZATION PATTERN

18CSM21015A

SIZE	DWG. NO	REV. LTR
C	18CSM21015 A	

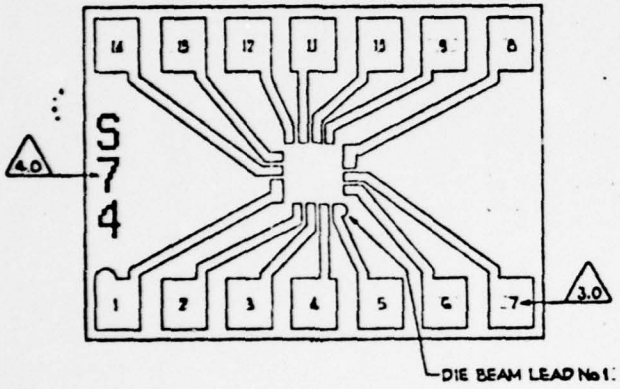


BEAM BOND PADS

ALL DIMENSIONS ARE BASIC

SCALE 60/1

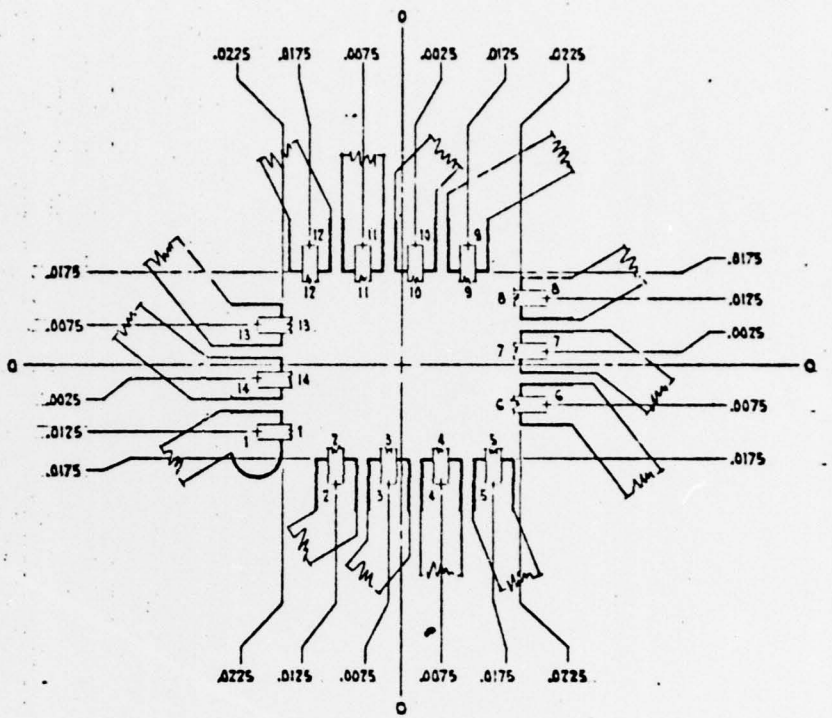
PART No A009



METALLIZATION PATTERN

18CSM21015A

SIZE C DWG NO 18CSM21015 A

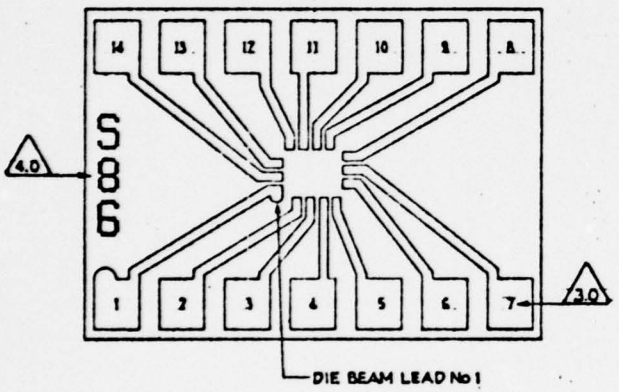


BEAM BOND PADS

ALL DIMENSIONS ARE BASIC

SCALE 60/1

18CSM21015 A



METALLIZATION PATTERN

PART No A010

SIZE C | DWG NO 18CSM21015 A | REV LTR